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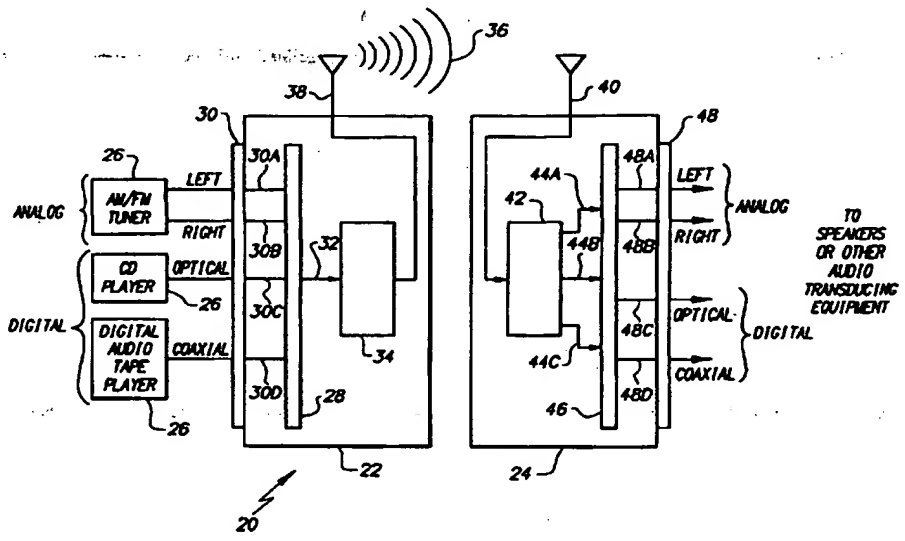

(57) Abstract

This invention discloses a digital wireless speaker system (20) for use in consumer audio applications. A digital radio frequency transmitter (22) is connected to an analog or digital audio source (26) and a digital radio frequency receiver (24) provides for reception of the transmitted audio information in remote locations. In addition, the digital receiver (24) will be able to receive control information to implement such things as volume, tone controls, or other auxiliary information. This allows the user to listen to high quality audio in a variety of locations without the need of independent stereos or external wires. The system is based on digital circuitry to improve the performance of the system and provide for compact disc quality sound. The digital circuitry (34 and 42) incorporates forward error correction techniques and interleaving to enable the system (20) to account for errors in transmission and thus improve the overall performance of the system.

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DIGITAL WIRELESS SPEAKER SYSTEM

SPECIFICATION

FIELD OF THE INVENTION

The invention relates generally to the transmission and reception of information such as analog or digital audio data over the air. More particularly, the invention pertains to the transmission/reception of high fidelity audio signals over the air over short distances using high frequency carriers at low power.

BACKGROUND OF INVENTION

A number of systems have been developed to avoid wiring stereo speakers directly to the source of signals used to drive the speakers, e.g., phonographs, tape decks, CD players, or AM/FM tuners. By way of example, U.S. Patent No. 4,829,570, issued to Larry Schotz on May 9, 1991, discloses a system of this type. This system, while not requiring direct wiring between the source of signals and the speaker, transmits the signals over the A.C. electrical conductors of the building in which the system is located. The signals transmitted in this manner are subject to certain undesirable effects, such as filtering for computer systems. This type of filtering may eliminate or degrade the signals intended for transmission to the speakers.

An alternative to using any form of wiring between a speaker and the source of signals for driving the speaker is to transmit the signals over the air via electromagnetic waves such as radio waves. This type of system requires the use of a transmitter for transmitting the signals, a receiver for receiving the signals at the speaker, and a power amplifier for amplifying the signals at the speakers to properly drive the speakers. The drawback with this type of system is that the FCC strictly regulates the frequencies at which information may be transmitted over the air without the requirement of an appropriate license. Additionally, the number of frequencies at which transmission may occur is limited. Currently, the frequency bands available for transmitting information using low power transmission without a license are at high frequency

ranges. For example, the FCC currently allows the use of low power transmission (i.e., below 1 milliwatt for conventional modulation or below 1 watt for spread spectrum modulation, 47 CFR §15.249) in the range of 902 to 928 MHz, 2.4 to 2.483 GHz and 5.725 to 5.875 GHz. One such wireless speaker system is disclosed in U.S. Patent No. 5,299,264 (Schotz et al.) issued on March 29, 1994 and which is also assigned to the same assignee as the present invention.

Wireless speaker systems are desirable, since wiring is not required between the speakers and source of signals for driving the speakers; however, an arrangement of this type is not practical if the quality of the information signal driving the speaker is poor. Stereo speaker applications require high signal-to-noise ratios, good frequency response, low distortion, and stereo capability (simultaneous transmission of two channels of information) to be practical. A wireless speaker system is not a replacement for a system using wires unless the quality of information signals provided to drive the speakers results in a sound at the speakers comparable with the sound at similar speakers in a system using wires.

In addition, many compact disc players and digital audio tape players provide digital audio data output outlets, as well as analog audio data output outlets. In many instances, the speakers are hard-wired to the analog audio output outlets, rather than the digital audio output outlets. The problem with this is that the compact disc players and digital audio tape players process the audio signal digitally and then must convert the audio signal back to an analog signal for transmission over the speaker wire for ultimate use by the speaker. Such digital to analog conversion introduces additional signal distortion at the player before transmission on the line. It would be desirable to directly use the digital version of the audio signal (available at the digital audio data output outlets), thereby keeping distortion to a minimum, and then making the digital to analog conversion as close to the speaker as possible, after transmission is completed.

The transmission/reception of audio signals, e.g., music, (approximately 20 Hz to 20 kHz) must be distinguished from the transmission/reception of voice signals (approximately 300 Hz to 3 kHz). The former requires wideband transmission while the latter requires only narrowband transmission. Furthermore, where the transmission/reception of audio signals is accomplished using digital techniques, the transmission bandwidth must be further widened based on audio source sampling frequency, the standard use of two channels for audio, the number of bits per channel and any encoding process. These factors can easily require a 12 MHz transmission bandwidth, for example.

Accordingly, the need exists for a system capable of transmitting and receiving audio over the air using high frequency carriers at low power while maintaining the quality of the audio.

OBJECTS OF THE INVENTION

Accordingly, it is the general object of this invention to provide an apparatus which overcomes the disadvantages of the prior art.

It is still a further object of this invention to enable the user to listen to high quality audio in any remote location without external wires or independent equipment.

It is even yet a further object of this system to provide the user with compact disc quality sound through a wireless system.

It is yet a further object of this invention to provide, through the use of digital processing, a wireless speaker system that achieves performance similar to that found in top quality audio products.

It is still yet another object of this invention to provide a system that can directly transmit the digital audio data output available from compact disc players, digital audio tape players and any other digital audio sources.

It is yet another object of this invention to provide a system that can directly transmit the analog audio output available from compact disc players, digital audio tape players, as well as other sources.

It is yet a further object of this invention to provide a system for determining when the received audio data is invalid and muting that audio data until the validity of the audio data is restored.

It is yet a further object of this invention to provide a system for interpolating or muting the analog audio output whenever the received audio data is invalid.

SUMMARY OF THE INVENTION

These and other objects of the instant invention are achieved by providing a high fidelity, wireless transmission, audio system for use with a plurality of audio sources (e.g., an AM/FM tuner, a CD player, a digital audio tape player), each source providing a respective audio input signal. The audio system is arranged for wirelessly transmitting over the air an electrical signal representing one of the respective audio input signals. The audio system comprises a transmitter that is arranged to be coupled to a plurality of audio sources. The transmitter comprises an input means for selecting and converting one of the respective audio input signals into a first digital serial bit stream signal, a forward error correction encoding means for encoding the first digital serial bit stream signal to produce an encoded digital serial bit stream signal, a convolutional interleaving means for interleaving the encoded digital serial bit stream signal and for introducing a sync signal therein to form a second digital serial bit stream signal. The transmitter further comprises a carrier signal producing means for producing a carrier signal of a predetermined frequency of at least 2.4 GHz, a digital modulation means for modulating the carrier signal with the second digital serial bit stream signal to produce a modulated carrier signal and a first antenna means for emitting over the air the modulated carrier signal at a power level not exceeding approximately 1 milliwatt. Finally, the audio system comprises a receiver located within a range of approximately 10 to 300 feet (3 to 90 meters) of the transmitter and being coupled to an audio transducing device (e.g., a speaker). The receiver

demodulates the modulated carrier signal into a audio output signal.

DESCRIPTION OF THE DRAWINGS

Other objects and many of the attendant advantages of this invention will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings wherein:

Fig. 1 is a diagram of the digital wireless transmission system;

Figs. 2A and 2B together illustrate a block diagram of the transmitter of the digital wireless speaker system;

Figs. 3A and 3B together illustrate a block diagram of the receiver of the digital wireless speaker system;

Figs. 4A and 4B together illustrate a block diagram of the transmitter of the digital wireless speaker system using frequency hopping spread spectrum modulation;

Figs. 5A and 5B together illustrate a block diagram of the receiver of the digital wireless speaker system using frequency hopping spread spectrum demodulation;

Figs. 6A and 6B together illustrate a block diagram of the transmitter of the digital wireless speaker system using direct sequence spread spectrum modulation; and

Figs. 7A and 7B together illustrate a block diagram of the receiver of the digital wireless speaker system using direct sequence spread spectrum demodulation.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now in detail to the various figures of the drawing wherein like reference characters refer to like parts, there is shown at 20 in Fig. 1, the digital wireless speaker system.

The system 20 comprises a transmitter 22 and a receiver 24, each utilizing respective digital audio circuitry. Audio source equipment 26 (e.g., AM/FM tuner, phonograph, compact disc player, digital audio tape player, etc.) are coupled to the transmitter 22 via coupling means 30. The audio source equipment 26 provide audio input signals, in either analog or

digital format, via coupling means 30 to input means 28. In particular, analog left and right audio channel signals are accommodated on input lines 30A and 30B, respectively, while a digital optical audio signal is accommodated on an optical input line 30C; a digital audio signal is accommodated on a coaxial input line 30D. Among other things, the input means 28 also allows the user to select which audio source equipment 26 input signal on input lines 30A-30D is to be transmitted to the remotely located receiver 24, as will be discussed in detail later. The input means 28 also converts any analog audio input signals into digital format.

It should be noted that although Fig. 1 shows a CD player having an optical output and a digital audio tape player having a coaxial output as being coupled to the transmitter 22, each audio source has both optical and coaxial outputs; for simplicity, only one of the two types of outputs was depicted for each audio source.

Once a particular audio input signal has been selected, and converted to a digital format (if not in a digital format already), the transmitter digital audio circuitry 34 processes that selected signal which is available on digital input line 32. The digital audio circuitry 34 basically modulates a 2.4 GHz carrier frequency signal with the selected audio input signal and prepares a broadcast signal 36 for transmission to the receiver 24. The broadcast signal 36 is transmitted from the transmitter antenna 38 and over the air to the receiver 24.

The receiver 24, located at a remote site (e.g., another room, floor level, etc., in the range of approximately 10 to 300 feet from the transmitter 22), receives the broadcast signal 36 via a receiver antenna 40. The receiver's digital audio circuitry 42 then demodulates the audio information from the broadcast signal 36 into respective digital output signals on lines 44A, 44B and 44C that are provided to an output means 46. The output means 46 provides the particular signal format, digital or analog, via audio output lines 48A, 48B, 48C or 48D to a coupling means 48 for connection to speakers or other audio transducing equipment.

The details of the transmitter 22 will now be discussed. As shown in Fig. 2, the input means 28 comprises anti-aliasing filters 50A and 50B, a 16-bit stereo A/D converter digital filter 52, a switching means 54, an optical digital receiver 56, a coaxial digital line receiver 58, a clock synchronization circuit 60, a digital interface transmitter 62, a transmitter microprocessor (μP) 64 (or a digital signal processor, DSP) and a transmitter clock 66. At this juncture it should be noted that although the transmitter microprocessor 66 (e.g., EPROM-based 8-bit CMOS Microprocessor PIC16C55 or a digital signal processor, e.g., Motorola DSP56002) is shown in Fig. 2 as comprising a part of the switching means 54, the microprocessor 64 also forms a part of the phase-locked loop in the digital circuitry 34, to be discussed later. Although a separate, dedicated microprocessor could be used exclusively in the digital circuitry 34, the microprocessor 64 is capable of multi-purpose use within both the input means 28 and the digital audio circuitry 34. The anti-aliasing filters 50A and 50B process the left and right analog audio channel input signals, respectively, on input lines 30A and 30B, respectively. The purpose of these filters is to reduce errors in the analog-to-digital conversion, which follows the aliasing filters. The filtered left and right analog audio input signals are then fed to the A/D converter 52 (e.g., Philips Semiconductor SAA7360 A/D converter) where they are converted to the digital I^2S format or some other digital format. The A/D converter 52 also incorporates a digital filter to further suppress any aliasing errors. The output from the A/D converter is typically referred to as a digital audio interface comprising three main signals: a word clock on line 68A, a word data on line 68B, and a word select on line 68C. These three signals are then fed to a first switching element of switching means 54, which will be discussed later.

The digital wireless speaker system 20 also accommodates direct digital input on audio input lines 30C and 30D. Digital audio outputs are commonly found on compact disc players and digital audio tape players as well as other sources. By using

this direct digital input feature, the digital audio information is not further degraded by having multiple analog-to-digital and digital-to-analog conversions, as often occurs in most conventional audio processing equipment where such digital inputs are used. In particular, the digital inputs to the system 20 can be either optical (line 30C) or coaxial (line 30D). A coaxial input means a digital audio signal that is available to the transmitter 22 through an RCA connector.

The optical input signal on line 30C and the coaxial input signal on line 30D are fed to respective line receivers 56 and 58. These line receivers 56 and 58 are required to convert the respective input signals to proper digital format for ultimate processing in digital circuitry 34. In particular, the optical signal on line 30C is fed to an optical digital receiver 56 (e.g., Shimadzu HK-3131-01) and outputted on line 70 while the coaxial input signal on line 30D is fed to a coaxial line receiver 58 (e.g., any conventional transformer network used in converting coaxial digital inputs) and outputted on line 72.

Depending on which digital audio source, an optical audio source or a coaxial audio source (i.e., a source having a digital audio signal available via an RCA connector), is coupled to the transmitter 22, the user sets the switching means 54 so that either the signal on line 70 or the signal on line 72 is coupled to the clock synchronization circuit 60 via signal line 74. The synchronization circuit 60 (e.g., Crystal Semiconductor CS8412 digital receiver) obtains the data clock from the selected incoming biphase-mark digital signal on line 74 and outputs a digital audio interface (I^2S baseband) comprising a word clock on line 76A, a word data on line 76B, and a word select on line 76C to the digital interface transmitter 62.

If an analog audio source (e.g., an AM/FM tuner) is coupled to the transmitter 22, the user, in setting the switching means 54 accordingly, couples the signals on lines 68A, 68B and 68C to the digital interface transmitter 62. On the other hand, if an optical or coaxial audio source is coupled to the transmitter 22, the user, in setting the switching means 54 accordingly,

couples the signals on lines 76A, 76B and 76C to the digital interface transmitter 62.

The digital interface transmitter 62 (e.g., Crystal Semiconductor's Digital Audio Interface Transmitter CS8402) provides for the interface between the A/D converter 52/clock synchronization circuit 60 and the serial data stream needed for transmission. The purpose of the digital interface transmitter 62 is to convert the digital audio interface (I^2S baseband) into one serial bit stream (S/PDIF) that can be transmitted. In addition, the digital interface transmitter 62 allows additional subcode information to be sent along with the digital audio information. This allows control codes for such things as volume and tone controls, and other auxiliary information, to be relayed along with the digital audio information. The subcode information is also used to determine if the digital audio information is valid data. The microprocessor 64 (or a digital signal processor) can be used to generate the needed subcode information and transmits this subcode information to the digital interface transmitter 62 via code line 75. The output of the digital interface transmitter 62 can support the AES/EBU, IEC 958, S/PDIF, and EIAJ CP-340 interface standards. The serial data out is biphase-mark encoded and is provided to the digital audio circuitry 34 on input line 32.

The switching means 54 comprises a first switching element 78, a second switching element 80, the microprocessor 64, user audio source select switch 82 and audio source frequency select switch 84. When the user couples a particular audio source to the transmitter 22, the user then sets the audio source select switch 82 to the corresponding audio source indication. In addition, the user also sets the audio source frequency select switch 84 that corresponds to the sampling frequency of that particular audio source. Setting these two switches transmits corresponding electrical signals to the microprocessor on lines 86 and 88, respectively. These signals allow the microprocessor 64 to configure the first switching element 78 (e.g., any conventional electric select switch) and the second switching element 80 (e.g., any conventional electric select switch) so

that only one set of the data word, clock and select on lines 68A, 68B and 68C or on lines 76A, 76B and 76C are coupled to the digital interface transmitter 62. The microprocessor 64 controls the switching elements 78 and 80 by signals on respective control lines 90 and 92. The audio source select switch 82 and the audio source frequency select switch 84 are located on the outside of the transmitter 22 unit.

The transmitter clock 66 (e.g., M2 Series D300 Voltage Controlled Oscillator) controls the digital sections of the transmitter 22. The clock 66 runs at 256 times the audio source sampling frequency which can be 32 kHz, 44.1 kHz, or 48 kHz. Thus, the transmitter clock 66 will be running at 8.192 MHz, 11.2896 MHz, or 12.288 MHz, respectively. The user selects one of these frequencies (corresponding to the audio source coupled to the transmitter 22) via the audio source frequency select switch 84. A control signal is transmitted from the switch 84 to the transmitter clock 66 on control line 94. The three different clock frequencies are used in order to be compatible with various sampling frequencies used in different digital audio source equipment. The required clocking signals for the A/D converter 52, the digital interface transmitter 62 and the digital audio circuitry 34 are all derived from this clock 66. The clock signals needed for these circuits are derived at by dividing the transmitter clock signal down, provided on clock line 96, to the desired frequency.

The details of the transmitter digital audio circuitry 34 will now be discussed. As also shown in Fig. 2, the digital circuitry 34 comprises a forward error correction (FEC) encoder 98, a data packet convolutional interleaver 100, a modulator 103 and an RF amplifier 108. The modulator 103 comprises an I-Q generator 102, a quadrature phase-shift keying RF modulator 104 and a local oscillator circuit 106. The encoder 98, interleaver 100 and the I-Q generator 102 operate in accordance with the transmitter clock 66.

Due to the RF properties of the system 20, errors in the digital transmission are likely to occur. Random noise and dropouts can cause serious data errors which result in poor

performance. To overcome this, the combination of forward error correction (FEC) and data interleaving is performed on the digital audio information. Forward error correction (FEC) is the only feasible correction method because an automatic repeat request (ARQ) system could not operate in real time. Thus, using the forward error correction (FEC) scheme, it is possible to send coded information so that the data at the receiver 24 can be corrected. In order to implement the FEC, an encoder/decoder IC by Space Research Technology will be used, whereby encoding is performed in the transmitter digital circuitry 34 and the decoding is performed in the receiver digital circuitry 42, which will be discussed later. The SRT241203 is a Hyper-Fec III CMOS Hard Decision Forward Error Correction Encoder/Decoder. This FEC encoder 98 utilizes extended Golay short block code to correct errors. The FEC decoder 198 (in the receiver digital circuitry 42, Fig. 3) can correct up to three random errors per codeword and it can detect up to four random errors in any codeword. The encoder 98/decoder 198 have a net coding gain of 3 dB at a BER (bit error rate) of 10^{-6}.

The FEC encoder 98/decoder 198 alone can only correct random errors and has little effect in helping burst errors. To overcome this, a data packet interleaver 100 and deinterleaver 200 (in the receiver digital circuitry 42) are used to provide for burst error correction. The interleaver 100 essentially takes the incoming encoded digital audio information on line 110 and combines it in such a fashion that no adjacent audio information is next to each other. The net result is that when a burst error does occur, only a few bits from each codeword are in error instead of the entire codeword. This allows the FEC encoder 98/decoder 198 to correct these errors in each codeword. The interleaver 100 simply spreads out the burst error over multiple codewords so that they can be corrected. The interleaver 100/deinterleaver 200 is based on Space Research Technology's SRT-24INT. The SRT-24INT utilizes a convolutional interleaving design which provides for faster and more efficient interleaving. In addition, the SRT-24INT is easier to implement in the digital circuities 34 and 42 because only one SRAM IC is

needed. Synchronization is also faster and easier using convolutional interleaving versus block interleaving. Furthermore, a sync signal is added to the serial data stream at this point which is later used by the deinterleaver 200 in the receiver 24 for synchronization.

It should be noted at this juncture that the applicant is developing a custom integrated circuit for the present invention in which resides both the FEC encoding and the data packet convolutional interleaving. The advantages of a single integrated circuit for housing the FEC encoding and interleaving include reduced circuit board space, reduced cost and reduced error in board wiring. Similarly, the applicant is also developing a custom integrated circuit for the present invention in which resides both the FEC decoding and the data packet convolutional deinterleaving for similar reasons.

The information being transmitted is digital and, therefore, a digital transmission method is implemented in the modulator 103 to improve performance. Quadrature Phase Shift-Keying (QPSK) is used for various reasons such as reduced bandwidth requirements and relatively easy implementation. The carrier frequency for the system 20 will be in the 2.4 GHz band for several reasons. First, interference in this band is significantly reduced relative to other bands. Second, the available bandwidth meets the transmission requirements. Lastly, at 2.4 GHz, the antenna size (i.e., transmitter antenna 38 and receiver antenna 40) is much smaller and less obtrusive to the user. As will be discussed later with respect to the local oscillator circuitry 106, several frequencies within the 2.4 GHz band can be selected from by the user.

At this juncture, it should be noted that although a quadrature phase-shift keying (QPSK) modulation scheme is disclosed herein, a binary-phase shift keying (BPSK) scheme could also be implemented in the modulator 103 using the similar hardware described below. Furthermore, a corresponding BPSK scheme could also be implemented in the receiver demodulator using the similar hardware described for the receiver demodulation stage 134, as will be discussed later.

The RF modulator 104 is based on RF Micro-Devices RF2422 QPSK modulator. The modulator 104 requires a separate I (in-phase) input and Q (quadrature) input. The interleaved serial input signal on line 112 is first divided into separate I and Q serial data streams on lines 114A and 114B, respectively. This is accomplished by the I-Q generator 102 which comprises a serial-to-parallel shift register (not shown) and a clocking signal from the transmitter clock 66. The I and Q signals are fed to buffer amps 116A and 116B, respectively, in the RF2422. The two buffered signals on lines 118A and 118B are then fed to respective mixers 120A and 120B which have local oscillator signals, on lines 122A and 122B, that are 90° out-of-phase. The outputs from the two mixers on lines 124A and 124B are then combined at another buffer stage 123. A Triquint TQ9132 RF power amplifier 108 is then used to boost the power of the signal for transmission as broadcast signal 36 via transmitter antenna 38. The broadcast signal 36 is emitted at a power level that is in compliance with 47 CFR §15.249, the FCC requirement for wireless transmission in the 2.4-2.483 GHz frequency band.

The local oscillator circuitry 106 comprises a local oscillator 126, a Phase-Locked-Loop (PLL) 128, a house code select switch 125 and the microprocessor 64. The local oscillator circuitry 106 produces any one of a number of carrier frequencies (e.g., 2.42 GHz, 2.44 GHz and 2.46 GHz). The user sets the house code select switch 125 (any variable position BCD switch that is located on the outside of the transmitter 22 unit) to a particular setting and this setting information is transmitted to the microprocessor 64 via data line 127. The microprocessor 64 then transmits the corresponding set of frequency data to the PLL 128 (e.g., Motorola MC12210 Serial Input PLL Frequency Synthesizer) on data line 129 which controls the local oscillator 126 (e.g., Z-Comm SMV2500 Voltage Controlled Oscillator) in generating the particular 2.4 GHz carrier frequency for the RF modulator 104. The local oscillator circuitry 106 is constructed in accordance with a similar transmitter local oscillator circuitry as disclosed in U.S. Application Serial No. 08/070,149, assigned to the same assignee

as this invention, namely L.S. Research, Inc., and whose disclosure is incorporated by reference herein. The only difference is that the local oscillator 128 operates in the 2.4 GHz range. The local oscillator output on line 130 is fed to a 90° carrier phase shift network 132 in RF modulator 104. This network 132 provides the two local oscillator signals, on lines 122A and 122B, that are 90° out-of-phase with respect to each other for mixing with the buffered signals on lines 118A and 118B, respectively.

The transmission frequencies of 2.42 GHz, 2.44 GHz and 2.46 GHz are exemplary only and are not meant to limit the present invention to those particular frequencies in the available 2.4 GHz band.

The details of the receiver 24 will now be discussed. As shown in Fig. 3, the receiver digital audio circuitry 42 comprises a demodulation stage 134 and a recombination-decode stage 136.

The demodulation stage 134 comprises a first bandpass (BFP) filter 138, a receiver front end 140, a second bandpass filter 142, a first local oscillator circuitry 144, a second local oscillator circuitry 146, a quadrature demodulator 148 and a carrier recovery circuit 150.

The incoming broadcast signal 36 is fed from the receiver antenna 40 to a bandpass filter 138 to filter out undesired signals. This first filtered signal is then fed on input line 152 to the input of a receiver front end 140 (e.g., HP MGA-86576 Low Noise RF Amplifier and IAM 81008 Mixer). The front end 140 is comprised of a low noise amplifier 154, an RF amplifier 156, and a mixer 158. The low noise amplifier 154 amplifies the first filtered signal which is then fed to a second bandpass filter 142 for further filtering and amplification by RF amplifier 156 to produce an RF signal on line 168 in preparation for demodulation.

The first local oscillator circuit 144 comprises a local oscillator 160 (e.g., Z-Comm SMV2500 Voltage Controlled Oscillator), a Phase-Locked-Loop (PLL) 162 (e.g., Motorola MC12210 Serial Input PLL Frequency Synthesizer), a receiver

microprocessor 164 and a house code select switch 165. At this juncture it should be noted that although the receiver microprocessor 164 (e.g., EPROM-based 8-bit CMOS Microprocessor PIC16C55 or a digital signal processor, e.g., Motorola DSP56002) is shown in Fig. 3 as comprising a part of the output means 46 (to be discussed in detail later), the microprocessor 164 also forms a part of the local oscillator circuit 144. Although a separate, dedicated microprocessor could be used exclusively in the output means 46, the microprocessor 164 is capable of multi-purpose use within the local oscillator circuit 144 and the output means 46. The first local oscillator circuit 144 is constructed in accordance with a similar receiver local oscillator circuit as disclosed in U.S. Application Serial No. 08/070,149, assigned to the same assignee as this invention, namely L.S. Research, Inc., and whose disclosure is incorporated by reference herein. The only difference is that the local oscillator 160 operates at 2.117 GHz. In particular, the user sets the house code select switch 165 (any variable position BCD switch located on the outside of the receiver 24 unit) to the corresponding setting of the transmitter house code select switch 125 and this setting information is transmitted to the microprocessor 164 via data line 167. The microprocessor 164 then transmits the corresponding set of frequency data to the PLL 162 on data line 169 which controls the local oscillator 160 in tuning the receiver to the particular 2.4 GHz carrier frequency of the incoming broadcast signal 36.

Once the local oscillator circuit 144 is set to the particular transmitter carrier frequency, a first local oscillator signal on line 166 is mixed with the RF amplifier signal on line 168 by mixer 158. This essentially performs the down-conversion from the 2.4 GHz carrier frequency to a first IF (intermediate frequency) for image rejection. This first IF signal, from the output of the mixer 158, is fed on line 170 to the second local oscillator circuitry 146.

The second local oscillator circuitry 146 performs a down-conversion on the first-IF signal to a second-IF signal. This second down-conversion is necessary to provide better adjacent

channel separation. The second local oscillator circuitry 146 comprises a first-IF amplifier 172, a mixer 174, a local oscillator 176 (e.g., a 255 MHz crystal oscillator), a 70-MHz bandpass filter 178 and a second-IF amplifier 180. In particular, the first-IF signal on line 170 is fed to the first-IF amplifier 172. This amplified first-IF signal is fed on line 174 to the mixer 176 and mixed with a local oscillator signal on line 182 that is set at 255 MHz. This mixing generates a second-IF signal on line 184 that is filtered by the 70 MHz bandpass filter 178 and then amplified by the second-IF amplifier 180. This amplified second-IF signal is transmitted on line 186 to the quadrature demodulator 148.

The quadrature demodulator 148 is an RF Micro-Devices RF2703 Quadrature demodulator. The demodulator 148 is comprised of a divide-by-two means 188 and two mixers 190A and 190B that, when used in conjunction with the carrier recovery circuit 150, demodulates the I and Q signals from the amplified second-IF signal. The carrier recovery circuit 150 is a frequency doubler that utilizes the filtered second intermediate frequency signal on line 151 to provide the requisite 140 MHz signal. The demodulated I and Q signals are then fed to recombination-decode circuit 136 on lines 192A and 192B, respectively.

The recombination-decoder circuit 136 comprises a data clock recovery circuit 194, an I-Q combiner 202, a convolutional deinterleaver 200 and an FEC decoder 198.

The data clock recovery circuit 194 (e.g., TRU050 Clock Recovery and Data Retiming Module) comprises an internal phase locked loop that locks onto the incoming I and Q signals present on input lines 192A and 192B. The data clock recovery circuit 194 then recovers a clock signal from the I and Q signals and provides a synchronized clock signal, along with the I and Q signals, to the I-Q combiner 202 on lines 196A, 196B and 196C, respectively. This synchronized clock signal is also fed forward to the deinterleaver 200 on line 203 for clocking-in the serial data from the I-Q combiner 202 on input line 206.

In the I-Q combiner 202, the demodulated I and Q signals, on input lines 196B and 196C, respectively, are recombined to

obtain a single serial digital data stream on output data line 206. In particular, the I-Q combiner 202 combines these signals using a parallel-to-serial shift register (not shown) and the synchronized clocking signal from the data recovery circuit 194.

Next, the received serial data on line 206 is deinterleaved by the deinterleaver 200 (e.g., the SRT-24INT, discussed earlier). Synchronization of the deinterleaver 200 is accomplished by utilizing the sync signal that was added to the serial data by the interleaver 100 in the transmitter 22. To assure that the incoming data is valid and synchronized, the deinterleaver 200 and the FEC decoder 198 work together. In particular, the decoder 198 checks the incoming data and clock from output lines 204A and 204B, respectively, to see if the deinterleaver 200 is synched. The decoder 198 then provides error reporting on status lines 208A and 208B back to the deinterleaver 200. If the data is invalid, the audio can either be interpolated or muted depending on the dropout time. If the data is valid, the FEC decoder 198 decodes the data, as described below. The ability of the deinterleaver 200 to hold sync, once acquired, is determined by the reliability of the interleaved data clock recovered at the receiving deinterleaver 200.

The FEC decoder 198 (e.g., the SRT241203, as discussed earlier) decodes the deinterleaved data and corrects any errors due to the RF transmission using the extended Golay short block code. The decoder 198 has the ability to locate and correct errors in the codewords in real time. The decoder 198 also provides outputs on the quality of the received codewords. Again, this error information is used to decide whether to interpolate the audio output or to mute it, as will be discussed below. The decoder 198 outputs digital audio signals on lines 44A, 44B and 44C to the output means 46.

The output means 46 comprises an optical digital transmitter 210, a coaxial digital line driver 212, a digital interface transmitter 214, a D/A converter 216, analog filters 218A and 218B and the receiver microprocessor 164.

In particular, an optical digital transmitter 210 (e.g., Optical Digital Transmitter Shimadzu HK-3131-03) and a coaxial digital line driver 212 (e.g., any conventional transformer network used for converting to coaxial digital format) are provided, on lines 44B and 44C, respectively, for converting the digital audio signals back into the particular optical and coaxial output format on output lines 48C and 48D, respectively. An optical output receptacle 220 and a coaxial output receptacle 222 are available for connection to external digital audio transducing equipment which comprise the requisite D/A converters, necessary for user listening. As stated earlier, by having the external audio equipment (not shown) provide the D/A means, the receiver 24 avoids multiple and unnecessary conversions which would only further degrade the quality of the audio signal.

The digital audio data on line 44A is fed into the digital interface receiver 216 (e.g., Crystal Semiconductor's CS8412 digital audio interface receiver). The digital interface receiver 216 performs the function of taking in the digital serial information and demultiplexing it. The digital interface receiver 216 has the ability to receive and decode audio data according to the AES/EBU, IEC 958, S/PDIF, and EIAJ CP-340 interface standards. The interface receiver 216 decodes the subcode information that provides control information and also provides information on the quality of the digital audio data that was received. The receiver microprocessor 164, being coupled to the digital interface receiver 214 via interface line 224, is used to read the subcode information and determine the control codes. The control codes are used to control the receive end controls such as volume or tone controls. In addition, the microprocessor 164 obtains the error information from the decoder 198 on status line 226 and the digital audio interface receiver 214 and determines whether or not to mute the audio output. The microprocessor 164 could also perform signal processing on the digital audio data to perform a variety of special effects such as digital surround sound.

The digital audio output from the digital interface receiver 214 is comprised of three signals: a word clock on line 228A, a word data on line 228B, and a word select on line 228C. These three signals are compatible with a variety of digital-to-analog converters.

The 16 bit stereo D/A converter/digital filter 216 (e.g., TDA1305T DAC) is used to perform the digital-to-analog conversion. The D/A converter 216 also incorporates an upsampling filter and a noise shaper which increases the oversampling rate significantly. This reduces the requirements of post analog filtering. The analog audio left and right outputs from the D/A converter 216, on lines 230A and 230B, respectively, are then filtered by simple first-order analog filters, 218A and 218B, respectively. The filtered analog left and right audio output signals are then available on output lines 44A and 44B, respectively.

Both the transmitter 22 and the receiver 24 have respective power circuits (not shown) that convert input power (e.g., 120VAC at 60 Hz) into proper voltage levels for appropriate transmitter and receiver operation.

It should also be noted at this point that a spread spectrum modulation technique, e.g., frequency hopping, direct sequence, time hopping or a hybrid of these three techniques, can be used in the system 20. Two exemplary spread spectrum techniques, a frequency hopping implementation (Figs. 4A-5B) and a direct sequence implementation (Figs. 6A-7B) are discussed below.

Due to the high bit rate involved in this system 20, in order to implement a practical spread spectrum modulation, audio compression/decompression must be implemented. To implement audio compression/decompression, the transmitter input means 28 and the receiver output means 46 must be modified.

As shown in Figs. 4A and 6A, the transmitter input means 28 has been modified to include audio compression. In particular, the digital interface transmitter 62 has been replaced with a MPEG (moving picture expert group) encoder 300 (e.g., SAA2520 stereo filter and codec/SAA2521 masking threshold

processor for layer 1 audio compression), and the microprocessor 64 has been replaced with a digital signal processor 302 (e.g., a DSP56002). The MPEG encoder 300 has the ability to provide a range of compression ratios. In this application, the compression ratio would provide for 384 kbit/sec given an audio input of 1.4 Mbit/sec. For this compression ratio, there is no subjective audio degradation compared to 16-bit PCM. The MPEG encoder 300 takes the digital audio interface output selected by the switch 80 and compresses that interface output into sub-band I^2S interface signals on line 304. The digital signal processor 302 then multiplexes the sub-band I^2S interface signals into a single serial bit stream while introducing synchronization preambles into the data stream. This serial bit stream is then outputted on the digital audio circuitry input line 32 where the bit stream is processed by the FEC encoder 98, the data packet convolutional interleaver 100 and the I-Q generator 102 in the same manner described previously. The MPEG encoder 300 is configured to perform layer 1 compression (basically, a simpler algorithm than layer 2). It should be noted that the MPEG encoder 300 and the digital signal processor 302 are coupled to the transmitter clock via clock lines 305 and 306, respectively. Furthermore, the digital signal processor 302 controls the switching means 54 and the PLL 128 in the same manner as described previously. In addition, the digital signal processor 302 also provides subcode information (e.g., volume and tone control) to be relayed with the digital information as stated previously with respect to the microprocessor 64.

As shown in Figs. 5B and 7B the receiver output means 46 has been modified to include audio decompression. In particular, the digital interface transmitter 214 has been replaced with a MPEG decoder 400 (e.g., SAA2520 stereo filter and codec for layer 1 audio compression), and the microprocessor 164 has been replaced with a digital signal processor 402 (e.g., a DSP56002). Both the digital signal processor 402 and the MPEG decoder 400 reverse the audio compression established in the transmitter 22. In particular, the digital signal processor 402 takes the decoded data from the output of the FEC decoder 198

on digital output signal line 44A and provides sub-band I^2S data (clock, data, select and error) on output lines 404A, 404B, 404C and 404D. The MPEG decoder 400 then decompresses this I^2S sub-band data into I^2S baseband data (word clock, word data and word select) on lines 228A, 228B and 228C, respectively, for processing the D/A converter 216, as discussed previously. Furthermore, the baseband I^2S data must be converted into S/PDIF format for use by the optical digital transmitter 210 and the coaxial digital line driver 212. As such, the word clock, word data and word select are fed on lines 229A, 229B and 229C, respectively, to the input of a digital interface transmitter 406 (e.g., CS8402) for conversion into S/PDIF format on output line 407, which in turn feeds the S/PDIF format signal to both the optical digital transmitter 210 and the coaxial digital line driver 212. Note that due to the need to decompress the audio, the decoded data output from the FEC decoder 198 is not fed directly to the optical digital transmitter 210 nor to the coaxial digital line driver 212, as discussed previously.

With frequency hopping spread spectrum modulation, a PN (pseudonoise) generator 308 has been added to the transmitter local oscillator circuit 106, as shown in Fig. 4B, to control the local oscillator 126. This modulation technique changes the carrier frequency at a constant rate within the 2.4 GHz band. Correspondingly, in the receiver 24, the reverse of this change is implemented. In particular, as shown in Fig. 5A, a PN code generator 408 along with a PN code synchronization circuit 410 have to be added to the receiver first local oscillator 144. The PN code synchronization circuit 410 output is fed to the oscillator 160 so that the receiver 24 can track the carrier frequency when it is hopping around.

With direct sequence spread spectrum modulation, a PN generator 312 and a mixer 314 have been added to the transmitter local oscillator circuit 106, as shown in Fig. 6B, to control the local oscillator 126. This modulation technique spreads the frequency of the carrier signal within the 2.4 GHz band. Correspondingly, in the receiver 24, the reverse of this change is implemented. In particular, as shown in Fig. 5A, a PN code

generator 412 along with a PN code synchronization circuit 414 have been added to the receiver first local oscillator 144. The PN code synchronization circuit 414 output is fed into a mixer 416 and mixed with the oscillator 160 output to de-spread the carrier frequency.

It should also be pointed out that use of spread spectrum modulation techniques in the 2.4 GHz band are allotted up to 1 watt of transmitting power rather than only the 1 milliwatt of power allotted for non-spread spectrum modulation. 47 CFR §15.249.

It should further be noted that although audio compression/decompression is necessary for implementing a practical spread spectrum modulation, both FEC encoding/decoding and data packet convolutional interleaving/deinterleaving may not be required for practical spread spectrum modulation. First, at higher transmitter power levels (as is allowed by the FCC for spread spectrum modulation) errors in the received signal are reduced. Second, where spread spectrum modulation is used, the transmitted signal is, in effect, spread out so that the carrier frequency is not residing at any one particular frequency during the transmission; as such, any interference from another signal using the same frequency at one point in time causes errors only in one portion of the transmitted signal rather than the entire signal. Therefore, the two exemplary spread spectrum techniques shown in Figs. 4A-7B could be depicted with neither FEC encoding/data packet convolutional interleaving in the transmitter digital audio circuitry 34 nor FEC decoding/data packet convolutional deinterleaving in the receiver recombination stage 136.

In particular, the input means 28 in Figs. 4A and 6A would generate a digital serial bit stream signal on digital audio circuitry input line 32 and then directly feed this signal to the I-Q generator 102 where it would be processed as described earlier and then modulated using spread spectrum techniques to produce a modulated carrier signal. Correspondingly, in the receiver 24, in Figs. 5B and 7B, once the modulated carrier signal is demodulated (using spread spectrum demodulation) and

converted into a single serial data stream signal by the I-Q combiner 202 on line 206, the data stream signal would be fed directly to the digital signal processor 400 on digital output signal line 44A.

Without further elaboration, the foregoing will so fully illustrate the invention that others may, by applying current or future knowledge, adopt the same for use under various conditions or service.

CLAIMS

1. A high fidelity, wireless transmission, audio system (20) for use with a plurality of audio sources (26), each source (26) providing a respective audio input signal, said audio system (20) arranged for wirelessly transmitting over the air an electrical signal (36) representing one of said respective audio input signals, characterized in that said audio system (20) comprises:

a transmitter (22) arranged to be coupled to said audio sources (26) and comprising:

input means (28) for selecting and converting one of said respective audio input signals into a first digital serial bit stream signal (32);

forward error correction encoding means (98) for encoding error correction into said first digital serial bit stream signal (32) to produce an encoded digital serial bit stream signal (110);

convolutional interleaving means (100) for interleaving said encoded digital serial bit stream signal (110) and for introducing a sync signal therein to form a second digital serial bit stream signal (112);

carrier signal producing means (106) for producing a carrier signal (130) of a predetermined frequency of at least 2.4 GHz;

digital modulation means (104) for modulating said carrier signal (130) with said second digital serial bit stream signal (112) to produce a modulated carrier signal (36);

first antenna means (38) for emitting over the air said modulated carrier signal (36) at a power level not exceeding approximately 1 milliwatt; and

a receiver (24) located within a range of approximately 10 to 300 feet (3 to 90 meters) of said transmitter (22) and being coupled to an audio transducing device, said receiver receiving and demodulating said modulated carrier

signal (36) into an audio output signal (48A, 48B, 48C and 48D).

2. The audio system (20) of Claim 1 characterized in that said receiver (24) comprises:

a second antenna means (40) for receiving said modulated carrier signal (36) radiated from said first antenna (38);

digital demodulation means (134) for demodulating said modulated carrier signal (36) into a demodulated digital signal (192A/192B);

data clock recovery means (194) for recovering a clock from said demodulated digital signal (192A/192B);

convolutional deinterleaving means (200) for deinterleaving said demodulated digital signal (192A/192B) in accordance with said sync signal to form a deinterleaved digital serial bit stream signal (204A/204B), said demodulated digital signal (192A/192B) being inputted to said deinterleaving means (200) in accordance with said clock;

forward error correction decoding means (198) for correcting errors in said deinterleaved digital serial bit stream signal (204A/204B) to form a digital audio signal (44A, 44B, 44C);

output means (46) for converting said digital audio signal (44A, 44B, 4C) into said audio output signal (48A, 48B, 48C and 48D) having a format compatible with the audio transducing device.

3. The audio system (20) of Claim 1 characterized in that said forward error correction encoding means (98) and said convolutional interleaving means (100) reside in a single integrated circuit.

4. The audio system of Claim 2 characterized in that said forward error correction decoding means (198) and said convolutional deinterleaving means (200) reside in a single integrated circuit.

5. The audio system (20) of Claim 1 characterized in that said input means (28) comprises a digital interface transmitter (62), said digital interface transmitter (62) receiving a digital audio interface input (68A, 68B, 68C or 76A, 76B, 76C) and converting said digital audio interface input (68A, 68B, 68C or 76A, 76B, 76C) into said first digital serial bit stream signal (32).

6. The audio system (20) of Claim 5 characterized in that said input means (28) further comprises a microprocessor (64), said microprocessor (64) transmitting subcode information to said digital interface transmitter (62) for introducing said subcode information into said first digital serial bit stream signal (32).

7. The audio system (20) of Claim 6 characterized in that said input means (28) further comprises switching means (54) for selecting one of said respective audio input signals to be processed by said digital interface transmitter (64).

8. The audio system (20) of Claim 1 characterized in that said one of said respective audio input signals comprises an analog left audio channel signal (30A) and an analog right audio channel signal (30B).

9. The audio system (20) of Claim 1 characterized in that said one of said respective audio input signals comprises an optical audio signal (30C).

10. The audio system (20) of Claim 1 characterized in that said one of said respective audio input signals comprises a digital audio signal (30D) from an RCA connector.

11. The audio system (20) of Claim 1 characterized in that said carrier signal producing means (106) comprises:

an oscillator (126);

a phase-locked loop (128);

a house code select switch (125); and

a microprocessor (64) having means for storing digital information representing a plurality of available carrier frequencies, said house code select switch (125) directing said microprocessor (64) to a portion of said digital information representing a particular carrier frequency and said

microprocessor (64) transmitting said portion to said phase-locked loop (128) for controlling said oscillator (126).

12. The audio system (20) of Claim 11 characterized in that said phase-locked loop (128) comprises a synthesizer, said synthesizer being connected to said oscillator (126), and having means for varying the frequency of said oscillator (126) to produce said carrier signal of a predetermined frequency of at least 2.4 GHz.

13. The audio system (20) of Claim 7 characterized in that said input means (28) further comprises an adjustable transmitter clock (66), said clock (66) being adjustable to correspond to said one of said respective audio input signals.

14. The audio system (20) of Claim 9 or Claim 10 characterized in that said input means (28) further comprises a clock synchronization circuit (60) for converting said optical audio signal (30C) or said digital audio signal (30D) from said RCA connector into a digital audio interface signal (76A, 76B, 76C).

15. The audio system (20) of Claim 2 characterized in that said digital demodulation means (134) generates a first intermediate frequency signal and a second intermediate frequency signal.

16. The audio system (20) of Claim 15 characterized in that said digital demodulation means (134) comprises:

a first oscillator (160);

a phase-locked loop (162);

a house code select switch (165); and

a microprocessor having means (164) for storing digital information representing a plurality of available carrier frequencies, said house code select switch (165) directing said microprocessor (164) to a portion of said digital information representing a particular carrier frequency and said microprocessor (164) transmitting said portion to said phase-locked loop (162) for controlling said first oscillator (160).

17. The audio system (20) of Claim 16 characterized in that said phase-locked loop (162) comprises a synthesizer, said synthesizer being connected to and having a means for varying the frequency of said first oscillator (160) to produce a first local oscillator signal (166).

18. The audio system (20) of Claim 17 characterized in that said digital demodulation means (134) further comprises a first mixer (158) for mixing said first local oscillator signal (166) with said modulated carrier signal (36) to generate said first intermediate frequency signal.

19. The audio system (20) of Claim 18 characterized in that said digital demodulation means (134) further comprises:

a second oscillator (176) of a constant frequency which produces a second local oscillator signal (182); and

a second mixer (174) for mixing said second local oscillator signal (182) with said first intermediate frequency signal to generate said second intermediate frequency signal (184).

20. The audio system (20) of Claim 1 characterized in that said digital modulation means (104) further comprises a quadrature-phase shift keying modulation means (104) for modulating said carrier signal (130) with said second digital serial bit stream signal (112).

21. The audio system (20) of Claim 1 characterized in that said digital modulation means (104) further comprises a binary-phase shift keying modulation means for modulating said carrier signal (130) with said second digital serial bit stream signal (112).

22. The audio system of Claim 2 characterized in that said forward error correction decoding means (198) comprises means for muting said deinterleaved digital serial bit stream signal (204A/204B) whenever said signal is invalid.

23. The audio system (20) of Claim 22 characterized in that said forward error correcting decoding means (198) further comprises means for transmitting error information to said output means (46).

24. The audio system (20) of Claim 23 characterized in that said output means (46) comprises a digital interface transmitter (214), said digital interface transmitter (214) receiving said digital audio signal (44A) containing subcode information and converting said digital audio signal into a digital audio interface signal (228A, 228B, 228C).

25. The audio system (20) of Claim 24 characterized in that said output means (46) further comprises a microprocessor (164), said microprocessor (164) receiving said error information for controlling said digital interface transmitter (214) to either interpolate or mute said digital audio interface signal 228A, 228B, 228C).

26. The audio system (20) of Claim 24 characterized in that said microprocessor (164) receives said subcode information from said digital interface transmitter (214) and controls said digital interface transmitter (214) to implement said subcode information into said digital audio signal (44A).

27. A high fidelity, wireless transmission, audio system (20) for use with a plurality of audio sources, each source providing a respective audio input signal, said audio system (20) arranged for wirelessly transmitting over the air an electrical signal (36) representing one of said respective audio input signals, characterized in that audio system (20) comprises:

a transmitter (22) arranged to be coupled to said audio sources (26) and comprising:

input means (28) for selecting, compressing and converting one of said respective audio input signals into a digital serial bit stream signal (32);

carrier signal producing means (106) for producing a carrier signal (130) of a predetermined frequency of at least 2.4 GHz;

spread spectrum modulation means (103) for modulating said carrier signal (130) with said digital serial bit stream (32) signal to produce a modulated carrier signal (36);

first antenna means (38) for emitting over the air said modulated carrier signal (36) at a power level not exceeding approximately 1 watt; and

a receiver (24) located within a range of approximately 10 to 300 feet (3 to 90 meters) of said transmitter (22) and being coupled to an audio transducing device, said receiver (24) receiving and demodulating said modulated carrier signal into an audio output signal (48A, 48B, 48C and 48D).

28. The audio system (20) of Claim 27 characterized in that said receiver comprises:

a second antenna means (40) for receiving said modulated carrier signal (36) radiated from said first antenna (38);

spread spectrum demodulation means (134) for demodulating said modulated carrier signal (36) into a demodulated digital signal (192A/192B);

data clock recovery means (194) for recovering a clock from said demodulated digital signal (192A/192B);

output means (46) for converting and decompressing said demodulated digital signal (192A/192B) into said audio output signal having a format compatible with the audio transducing device.

29. The system of Claim 27 characterized in that said input means (28) further comprises:

forward error correction encoding means (98) for encoding error correction into said one of said audio input signals to produce an encoded signal (110); and

convolutional interleaving means (100) for interleaving said encoded signal (110) and for introducing a sync signal therein to form a second digital serial bit stream signal (112).

30. The system of Claim 28 characterized in that said output means (46) further comprises:

convolutional deinterleaving means (200) for deinterleaving said demodulated digital signal (192A/192B) in accordance with said sync signal to form a deinterleaved digital serial bit stream signal (204A/204B), said demodulated digital signal (192A/192B) being inputted to said deinterleaving means (200) in accordance with said clock; and

forward error correction decoding means (18) for correcting errors in said deinterleaved digital serial bit stream signal (204A/204B) to form said audio output signal (48A, 48B, 48C and 48D);

31. The system (20) of Claim 27 characterized in that said spread spectrum modulation means (103) comprises frequency hopping modulation.

32. The system (20) of Claim 31 characterized in that said spread spectrum demodulation means (134) comprises frequency hopping demodulation.

33. The system (20) of Claim 27 characterized in that said spread spectrum modulation means (103) comprises direct sequence modulation.

34. The system (20) of Claim 33 characterized in that said spread spectrum demodulation (134) comprises direct sequence demodulation.

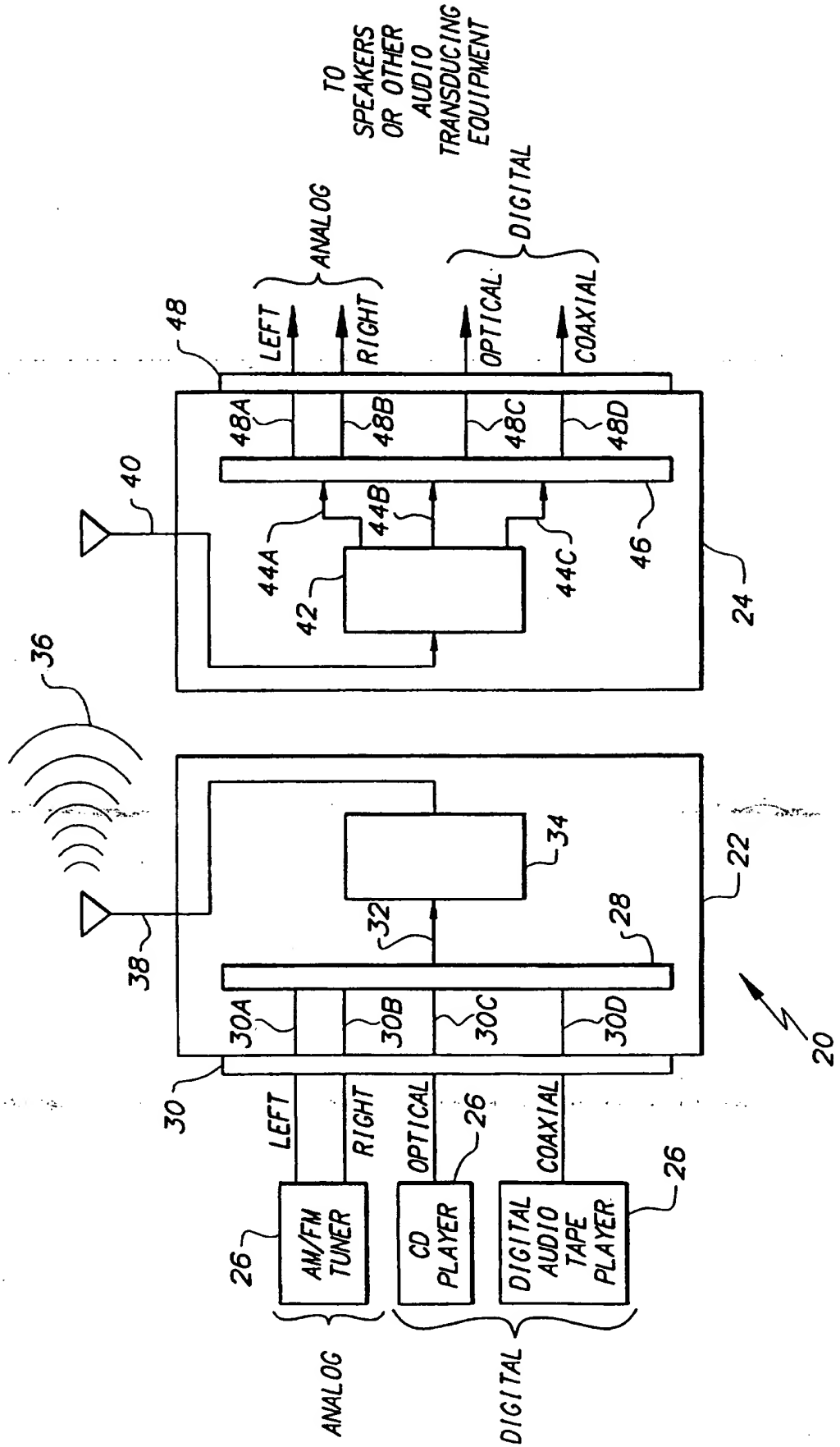

TO SPEAKERS OR OTHER AUDIO TRANSDUCING EQUIPMENT
ANALOG
DIGITAL
LEFT
RIGHT
OPTICAL
COAXIAL
48
48A
48B
48C
48D
40
44A
44B
44C
46
42
24
36
34
22
32
28
38
30A
30B
30C
30D
30
20
26
AM/FM TUNER
CD PLAYER
DIGITAL AUDIO TAPE PLAYER

FIG. 1

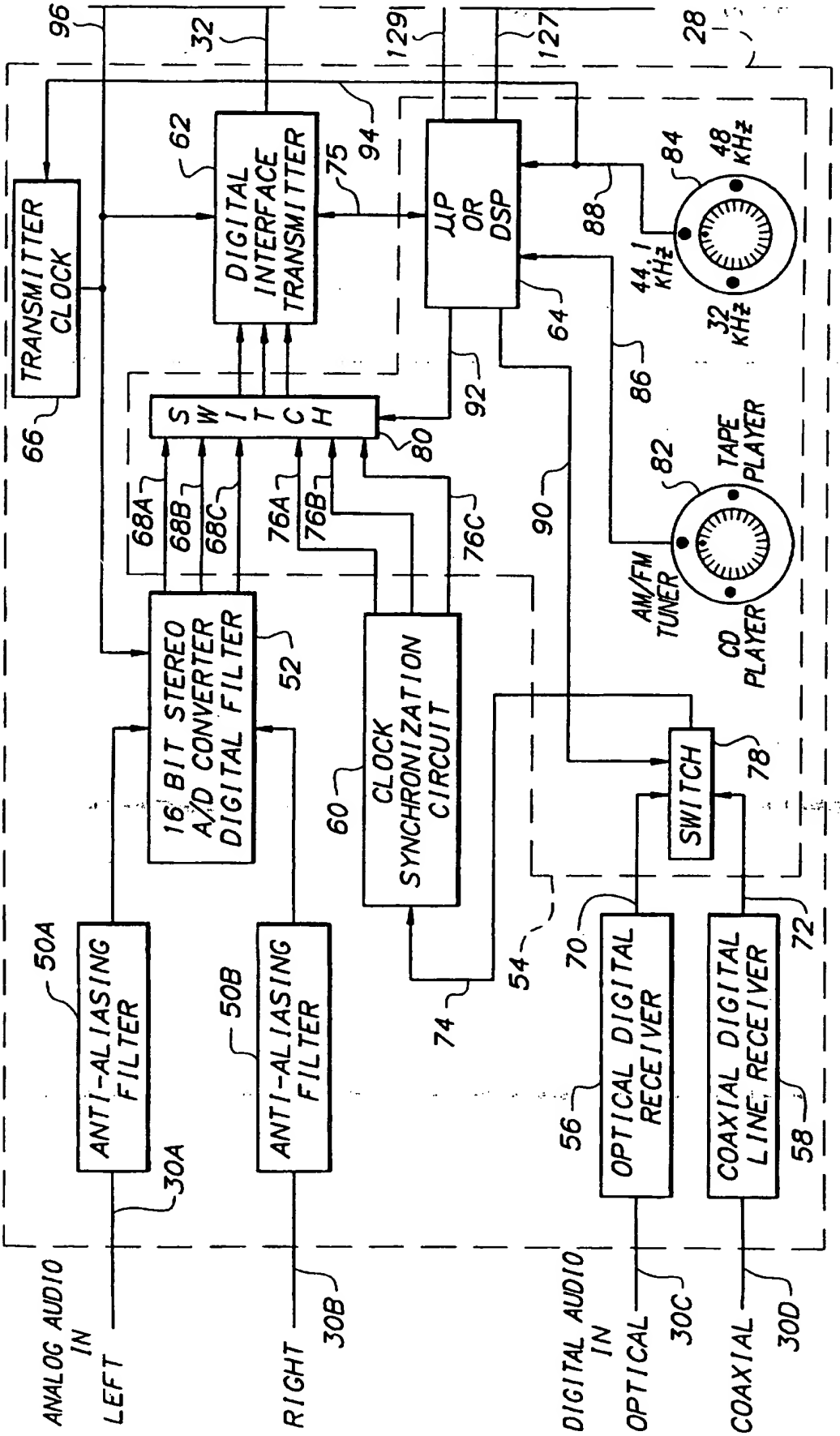


FIG. 2A

FIG. 2
FIG. 2A | FIG. 2B

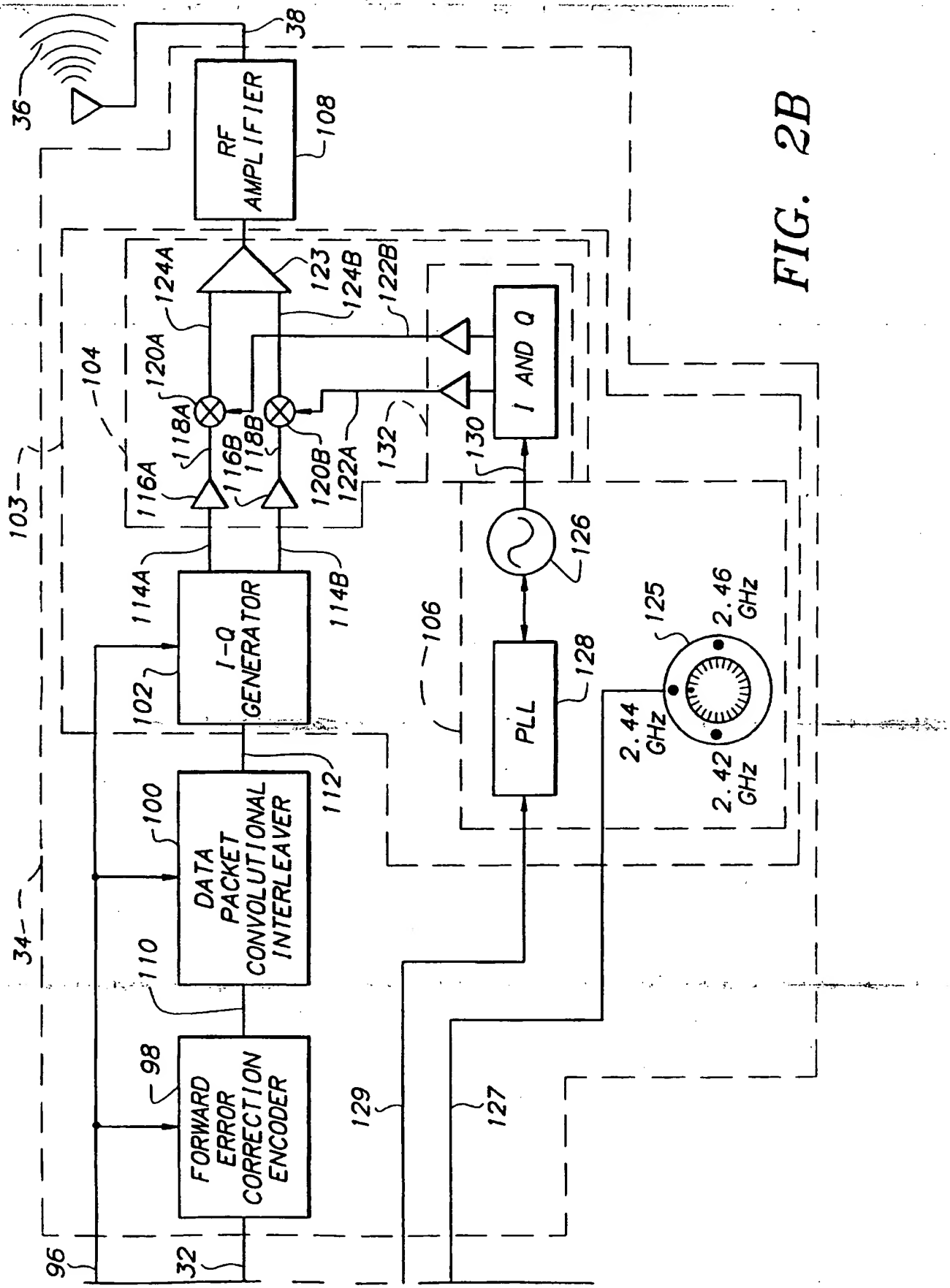

36
38
RF AMPLIFIER
108
123
124A
124B
122B
120A
104
118A
118B
116A
116B
120B
122A
132
130
I AND Q
103
126
114A
114B
I-Q GENERATOR
102
106
125
2.46 GHz
PLL
128
2.44 GHz
2.42 GHz
112
100
DATA PACKET CONVOLUTIONAL INTERLEAVER
34
110
98
FORWARD ERROR CORRECTION ENCODER
129
127
96
32

FIG. 2B

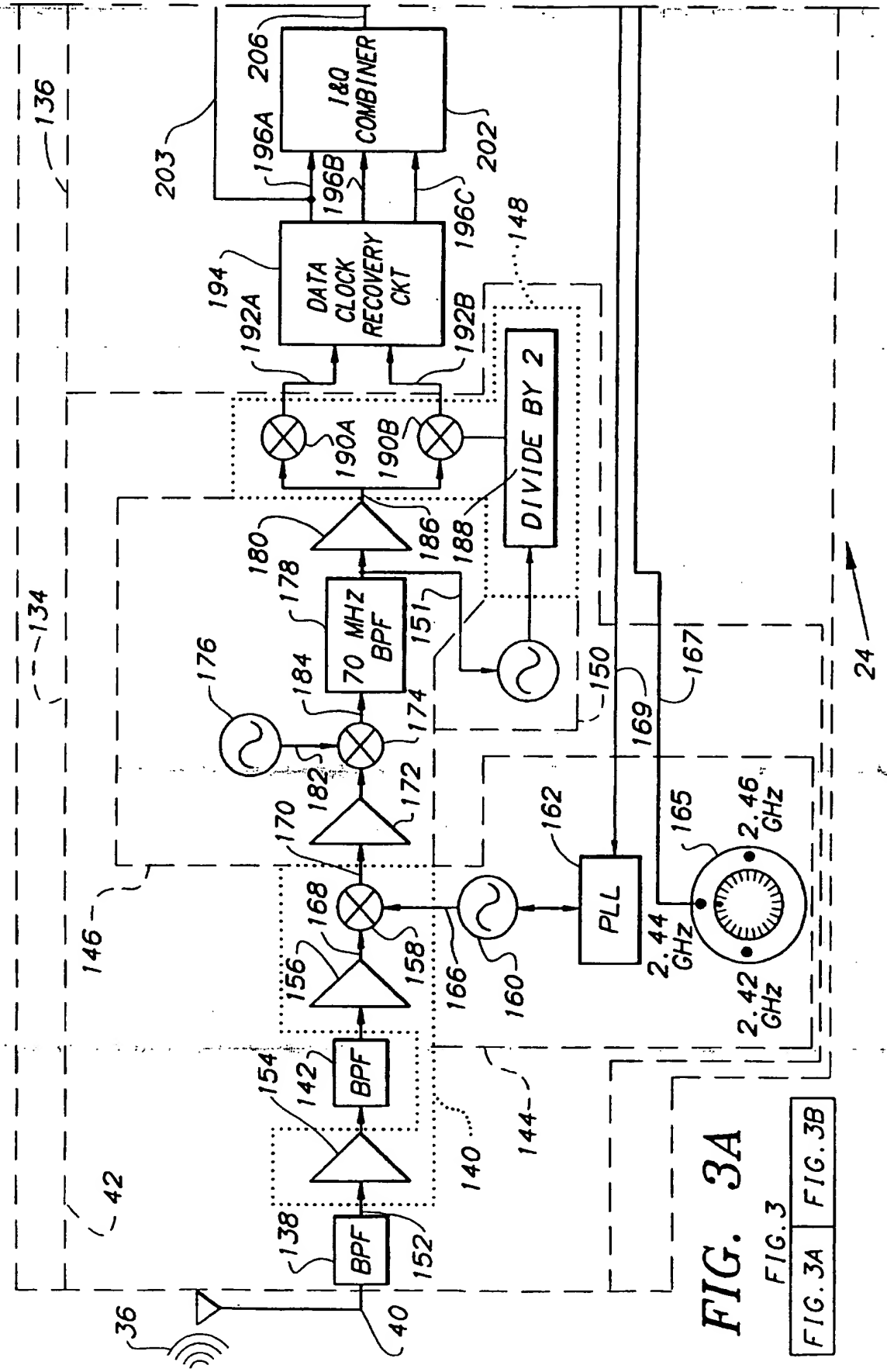
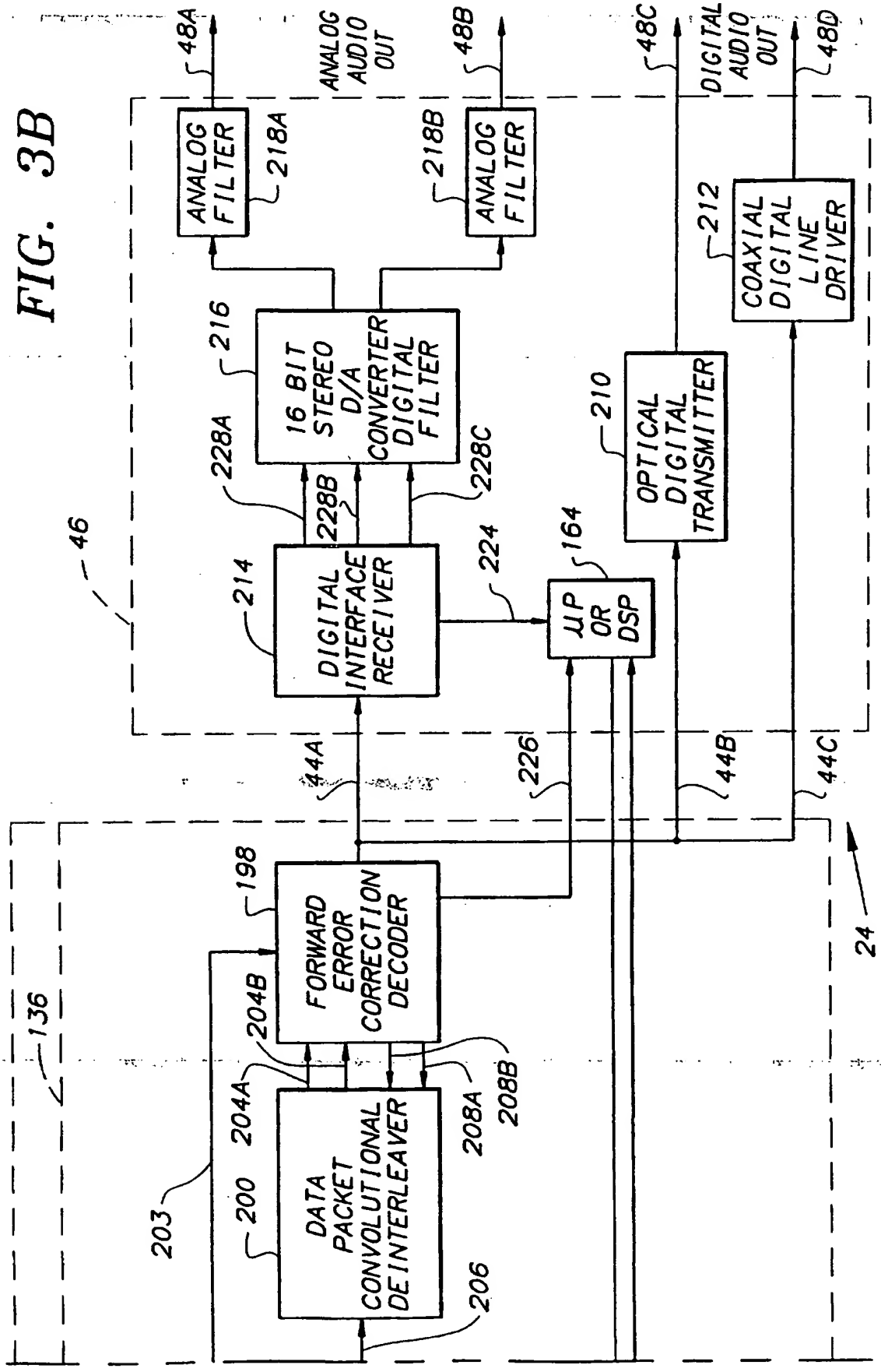


FIG. 3A

FIG. 3

FIG. 3A	FIG. 3B

FIG. 3B


48A
ANALOG AUDIO OUT
48B
48C
DIGITAL AUDIO OUT
48D
ANALOG FILTER
218A
218B
ANALOG FILTER
212
COAXIAL DIGITAL LINE DRIVER
216
16 BIT STEREO D/A CONVERTER DIGITAL FILTER
210
OPTICAL DIGITAL TRANSMITTER
228A
228B
228C
46
214
DIGITAL INTERFACE RECEIVER
224
164
µP OR DSP
44A
226
44B
44C
24
198
FORWARD ERROR CORRECTION DECODER
136
204B
204A
208A
208B
203
200
DATA PACKET CONVOLUTIONAL DEINTERLEAVER
206

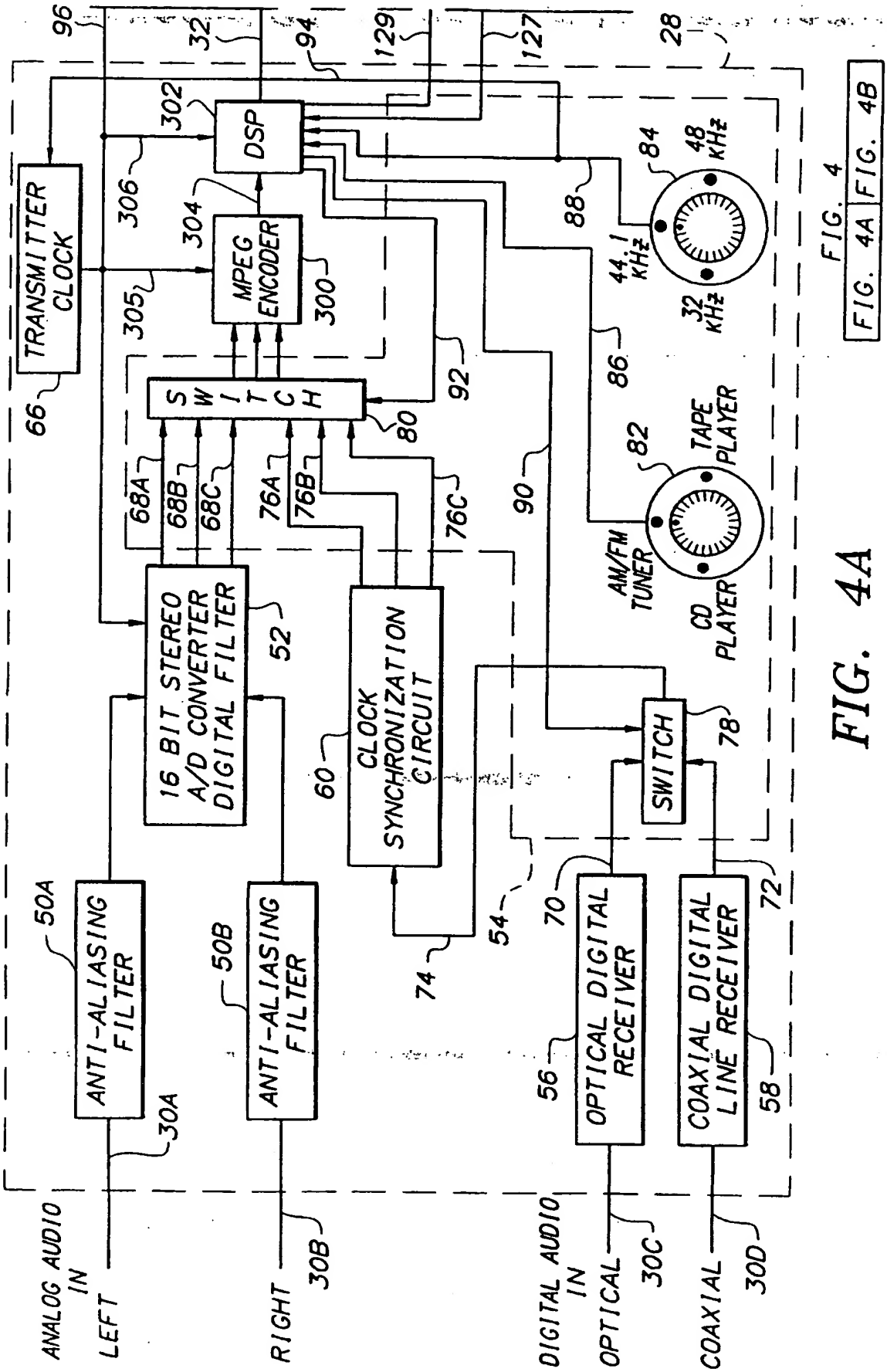


FIG. 4

FIG. 4A | FIG. 4B

FIG. 4A

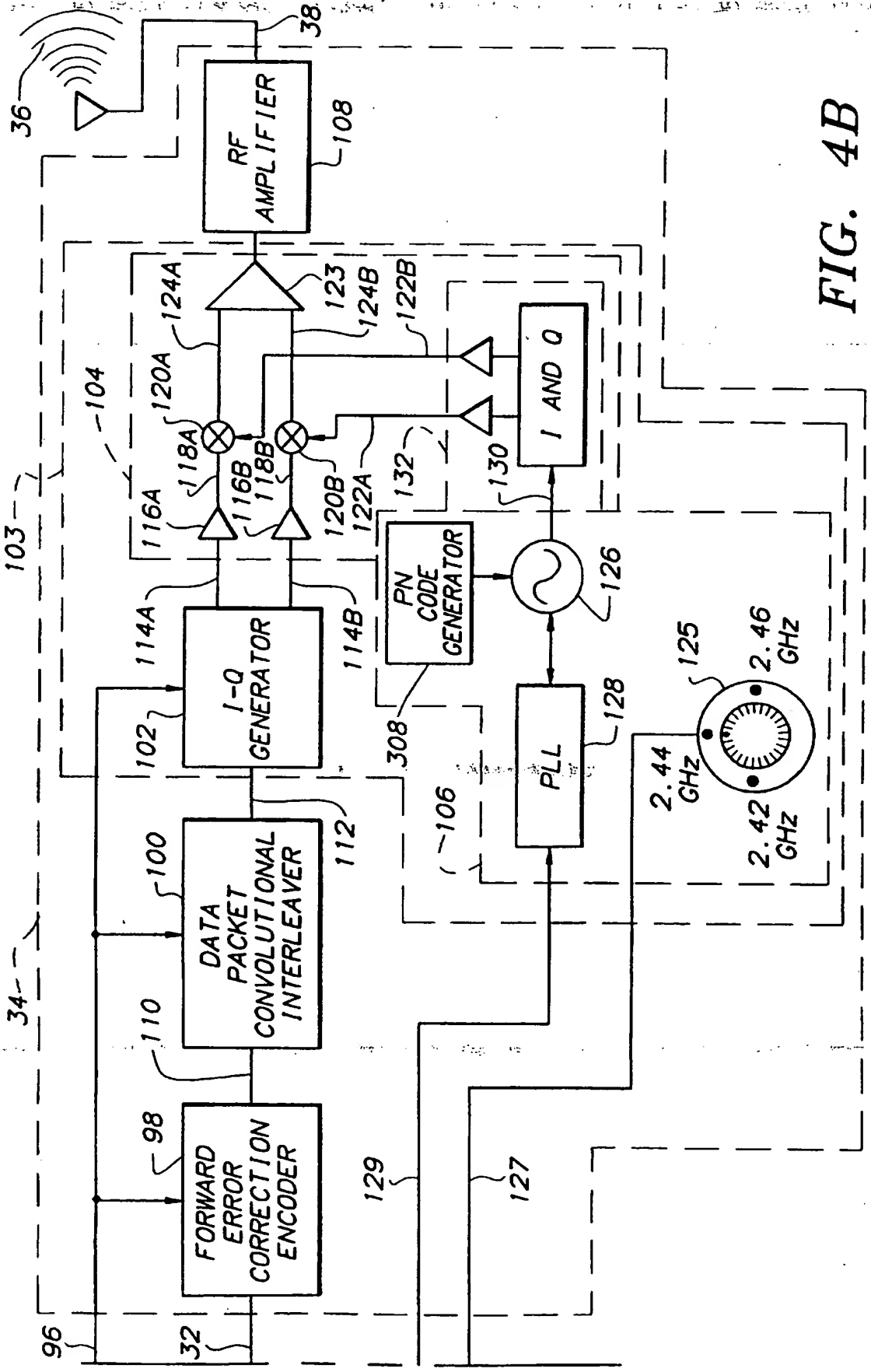

36
38
RF AMPLIFIER
108
123
124A
124B
122B
I AND Q
130
104
120A
118A
116B
118B
120B
122A
132
103
116A
PN CODE GENERATOR
126
114A
114B
I-Q GENERATOR
102
308
125
2.46 GHz
2.44 GHz
2.42 GHz
PLL
128
106
112
100
DATA PACKET CONVOLUTIONAL INTERLEAVER
34
110
98
FORWARD ERROR CORRECTION ENCODER
129
127
96
32

FIG. 4B

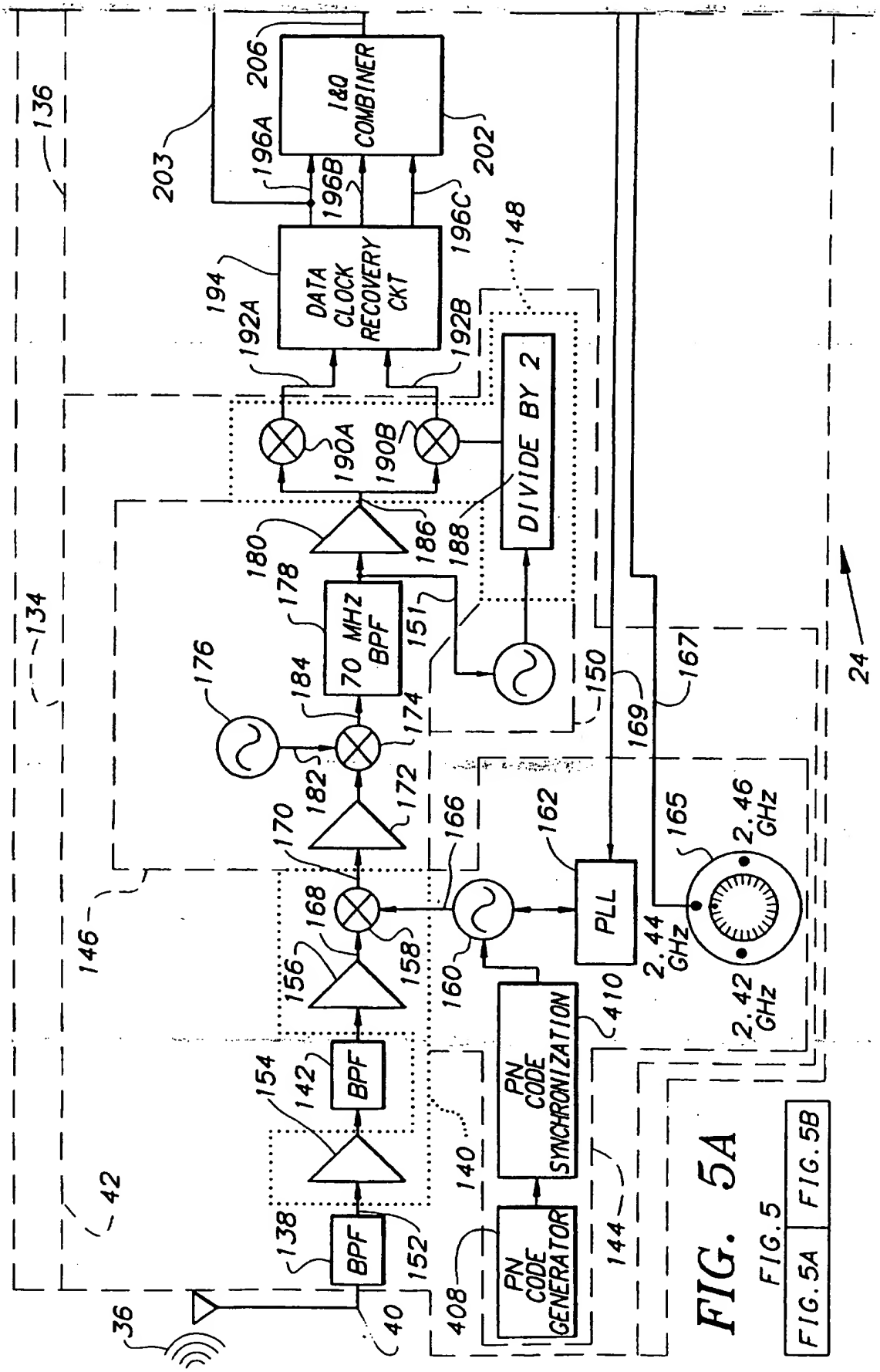
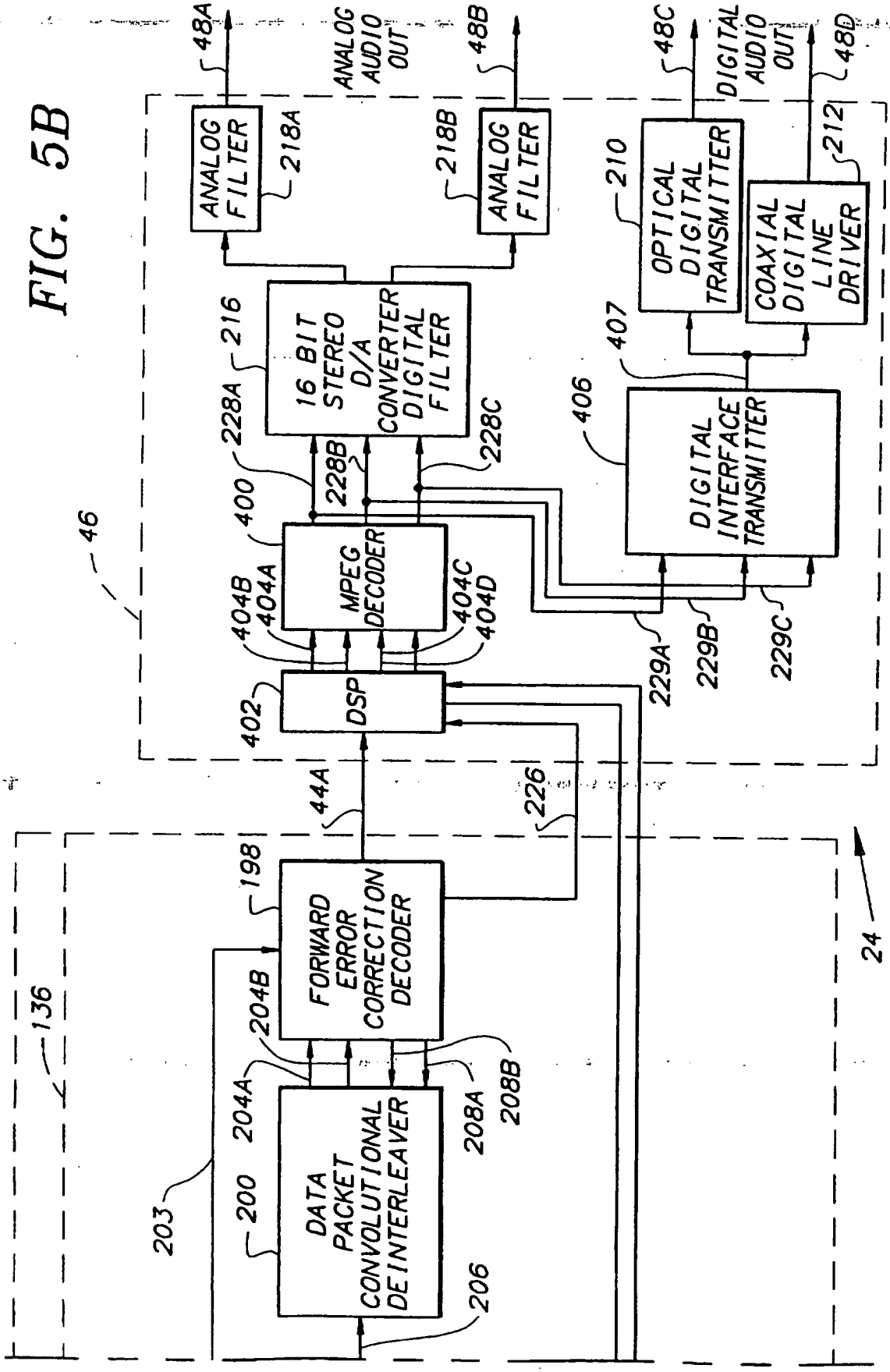


FIG. 5A

FIG. 5

FIG. 5A	FIG. 5B

FIG. 5B


48A
ANALOG AUDIO OUT
48B
48C
DIGITAL AUDIO OUT
48D
ANALOG FILTER
218A
218B
ANALOG FILTER
OPTICAL DIGITAL TRANSMITTER
210
COAXIAL DIGITAL LINE DRIVER
212
16 BIT STEREO D/A CONVERTER DIGITAL FILTER
216
228A
228B
228C
400
MPEG DECODER
404A
404B
404C
404D
DSP
402
DIGITAL INTERFACE TRANSMITTER
406
407
229A
229B
229C
46
44A
226
FORWARD ERROR CORRECTION DECODER
198
204A
204B
208A
208B
DATA PACKET CONVOLUTIONAL DEINTERLEAVER
200
206
203
136
24

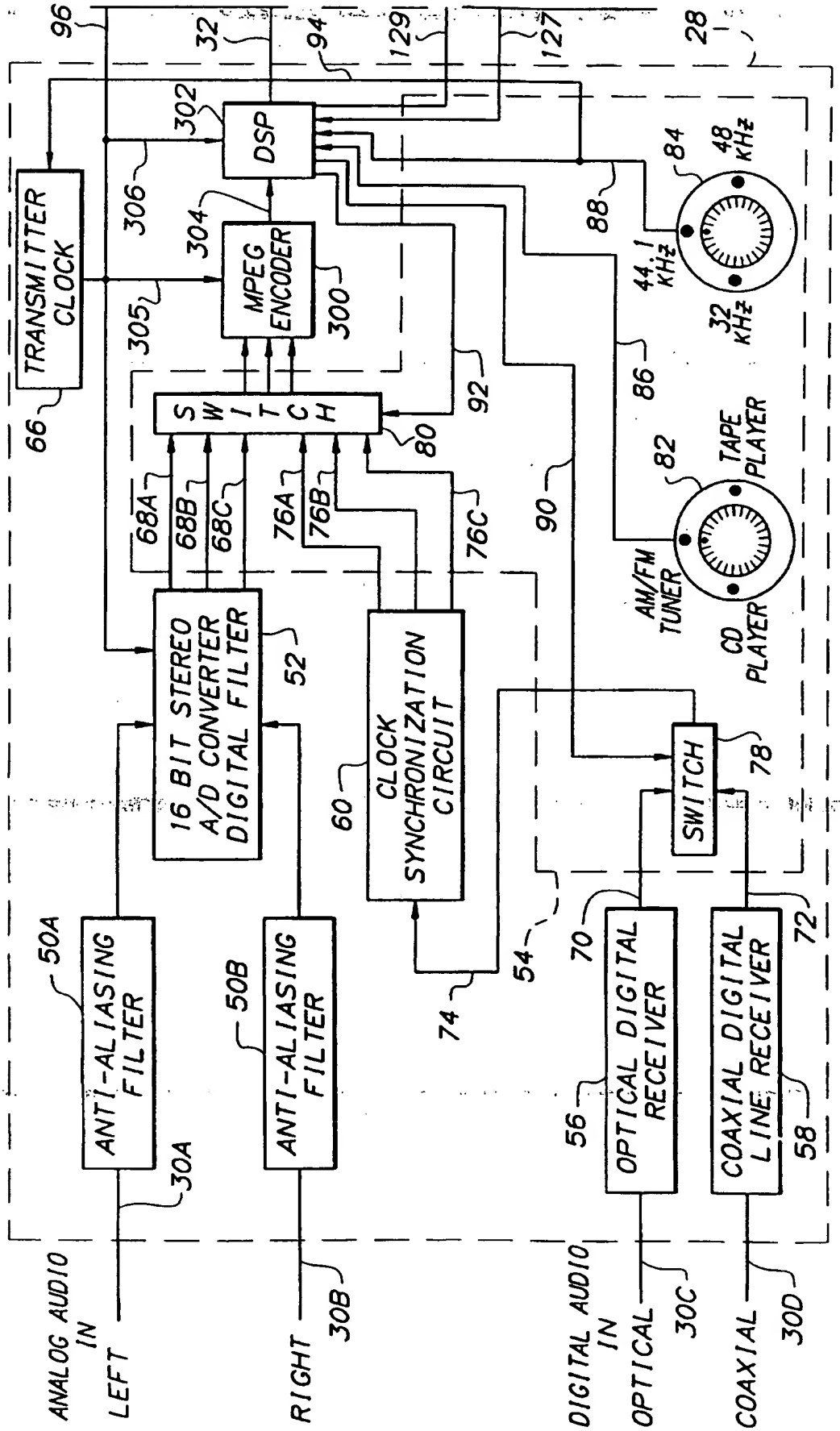


FIG. 6A

FIG. 6
FIG. 6A | FIG. 6B

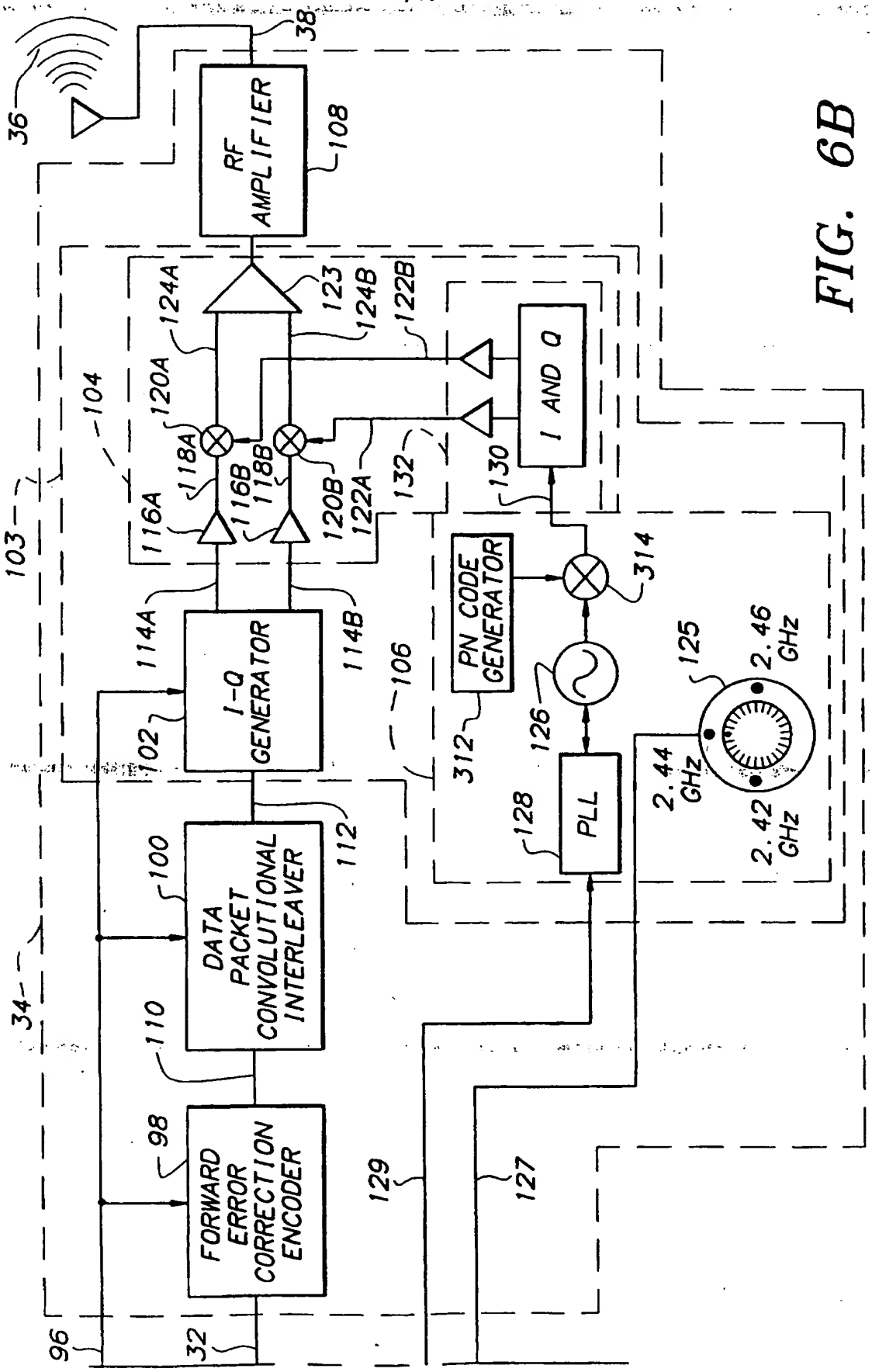

36
38
RF AMPLIFIER
108
123
124A
124B
122B
I AND Q
130
104
120A
118A
116B
118B
120B
122A
132
103
116A
PN CODE GENERATOR
314
114A
I-Q GENERATOR
114B
106
125
2.46 GHz
102
312
126
2.44 GHz
2.42 GHz
128
PLL
100
DATA PACKET CONVOLUTIONAL INTERLEAVER
112
34
110
98
FORWARD ERROR CORRECTION ENCODER
129
127
96
32

FIG. 6B

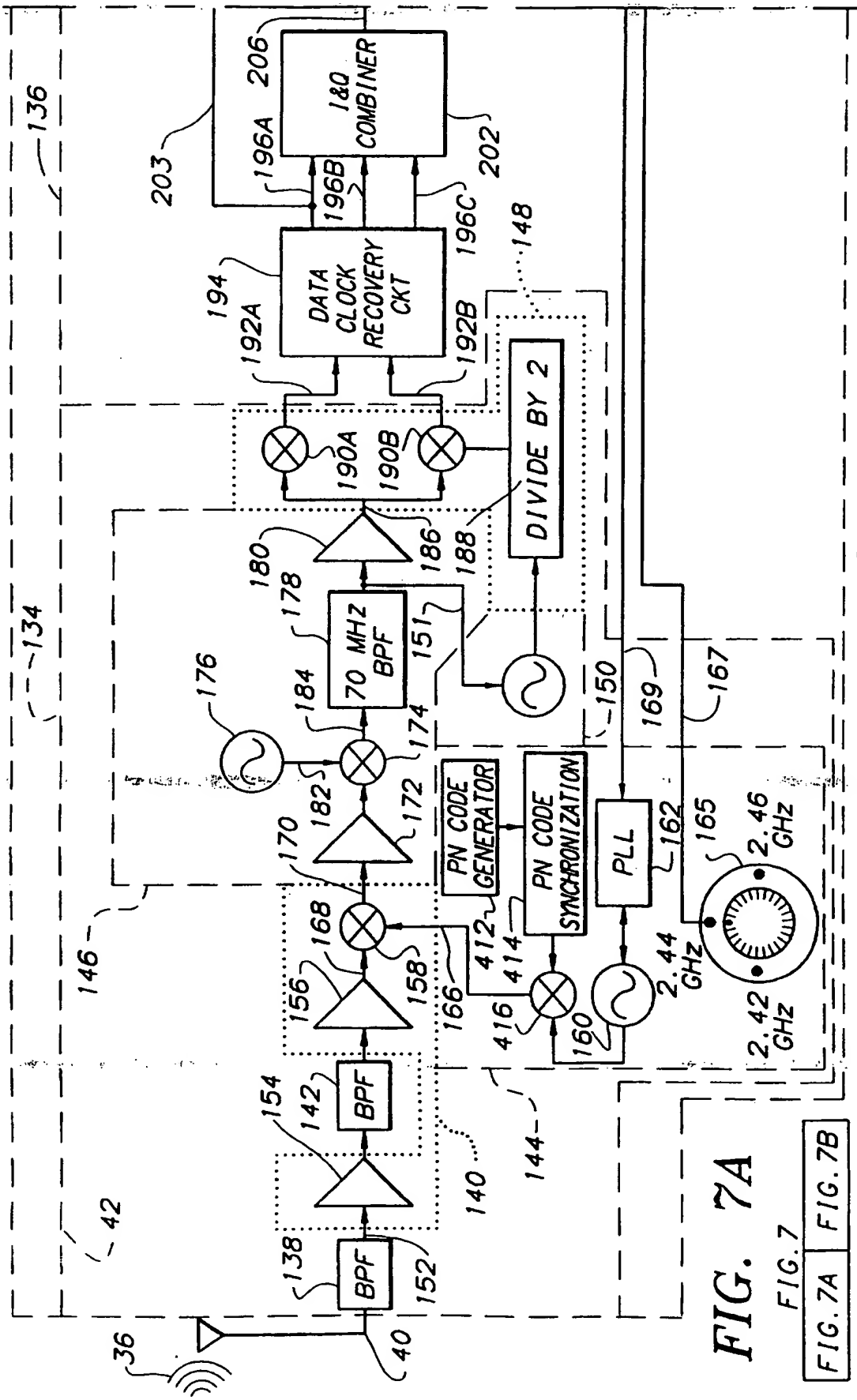
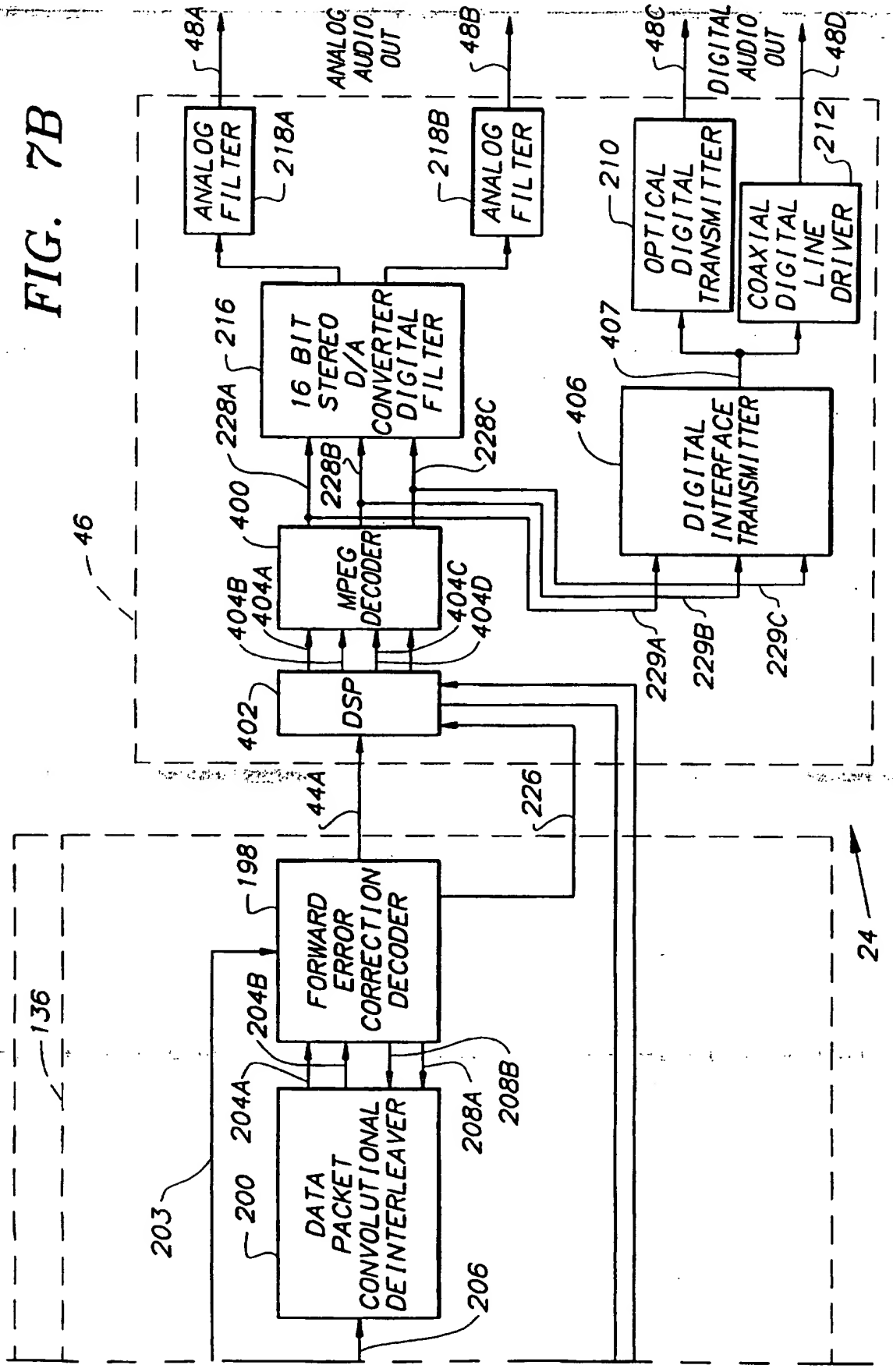


FIG. 7A

FIG. 7

FIG. 7A	FIG. 7B

FIG. 7B


48A
ANALOG AUDIO OUT
48B
48C
DIGITAL AUDIO OUT
48D
ANALOG FILTER
218A
218B
ANALOG FILTER
210
OPTICAL DIGITAL TRANSMITTER
212
COAXIAL DIGITAL LINE DRIVER
216
16 BIT STEREO D/A CONVERTER DIGITAL FILTER
228A
228B
228C
407
406
DIGITAL INTERFACE TRANSMITTER
46
400
MPEG DECODER
404B
404A
404C
404D
229A
229B
229C
402
DSP
44A
226
198
FORWARD ERROR CORRECTION DECODER
24
136
204B
204A
208A
208B
203
200
DATA PACKET CONVOLUTIONAL DEINTERLEAVER
206

INTERNATIONAL SEARCH REPORT

Interna l Application No
PCT/US 96/01648

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04B1/00 H04R5/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04B H04R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 299 264 A (SCHOTZ ET AL.) 29 March 1994 cited in the application see column 1, line 17 - column 4, line 38; figures ---	1,2,8, 11,12, 16-19, 22,27,28
Y A	US 4 621 374 A (MICIC ET AL.) 4 November 1986 see column 1, line 30 - column 3, line 44 ---	1,2,8, 11,12, 16-19,22 3-5,29
A	DE 44 18 337 A (MB QUART AKUSTIK UND ELEKTRONIK GMBH) 30 November 1995 see column 1, line 1 - column 3, line 35; figures --- -/--	1,6,9,10

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

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Date of the actual completion of the international search	Date of mailing of the international search report
14 March 1997	27. 03. 97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gastaldi, G

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INTERNATIONAL SEARCH REPORT

Interna] Application No
PCT/US 96/01648

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 94 28639 A (L.S. RESEARCH, INC.) 8 December 1994 see page 5, line 1 - page 7, line 18; figures	1,7,8
A	PRINCIPLES OF DIGITAL AUDIO, 1989, ISBN 0-672-22634-0, pages 185-228, XP002017123 KEN C. POHLMANN: "Chapter 8" see page 210 - page 228	1,30
Y A	US 4 941 150 A (IWASAKI) 10 July 1990 see column 1, line 6 - column 3, line 34; figures	27,28 33,34
A	WO 95 34960 A (VLSI TECHNOLOGY INC) 21 December 1995 see page 12, line 15 - line 23	31,32
A	PATENT ABSTRACTS OF JAPAN vol. 95, no. 010 & JP 07 288512 A (MATSUSHITA ELECTRIC IND CO LTD), 31 October 1995, see abstract	27
A	US 5 375 174 A (DENENBERG) 20 December 1994 see column 4, line 1 - line 16	27

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 96/01648

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

(See Annex)

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searches without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

FURTHER INFORMATION CONTINUED FROM PCT/ISA/210

Group I Claims 1-26 :
relates to a high fidelity, wireless transmission, audio system for use with a plurality of audio sources, the system having a transmitter comprising input means for selecting and converting one of the signals into a digital stream, forward error correction encoding means, convolutional interleaving means, carrier signal producing means for producing a carrier signal of a predetermined frequency of at least 2.4 GHz, digital modulation means, first antenna means for emitting at a power not exceeding 1 mW; and a receiver located within a range of approximately 3 to 90 meters of said transmitter and being coupled to an audio transducing device.

Group II Claims 27-34 :
relates to a high fidelity, wireless transmission, audio system for use with a plurality of audio sources, the system having a transmitter comprising input means for selecting, compressing and converting one of the signals into a digital stream, spread spectrum modulation means, carrier signal producing means for producing a carrier signal of a predetermined frequency of at least 2.4 GHz, first antenna means for emitting at a power not exceeding 1W; and a receiver located within a range of approximately 3 to 90 meters of said transmitter and being coupled to an audio transducing device.

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern. d Application No
PCT/US 96/01648

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5299264 A	29-03-94	CA 2119264 A	04-03-93
		EP 0600043 A	08-06-94
		US 5491839 A	13-02-96
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		AU 6957494 A	20-12-94
US 4941150 A	10-07-90	JP 63275233 A	11-11-88
WO 9534960 A	21-12-95	NONE	
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